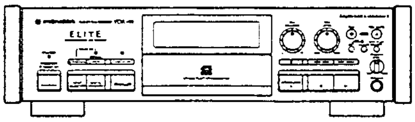
PIONEER®
The Art of Entertainment

Service Manual



ORDER NO.
RRV1280

COMPACT DISC RECORDER

PDR-99
PDR-05

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Type	Model		Power Requirement	Remarks
	PDR-99	PDR-05		
KU	○	○	AC120V	
ME8	-	○	AC220 - 230V	

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1. SAFETY INFORMATION

This service manual is intended for qualified service technicians; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.
Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING
Lead in solder used in this product is listed by the California Health and Welfare agency as a known reproductive toxicant which may cause birth defects or other reproductive harm (California Health & Safety Code, Section 25249.5).
When servicing or handling circuit boards and other components which contain lead in solder, avoid unprotected skin contact with the solder. Also, when soldering do not inhale any smoke or fumes produced.

NOTICE
(FOR CANADIAN MODEL ONLY)
Fuse symbols ■▭⊞ (fast operating fuse) and/or ■▭⊠ (slow operating fuse) on PCB indicate that replacement parts must be of identical designation.

REMARQUE
(POUR MODÈLE CANADIEN SEULEMENT)
Les symboles de fusible ■▭⊞ (fusible de type rapide) et/ou ■▭⊠ (fusible de type lent) sur CCI indiquent que les pièces de remplacement doivent avoir la même désignation.

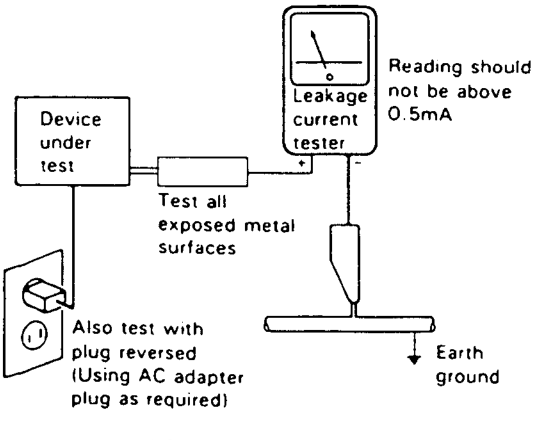
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.


Leakage current tester
Reading should not be above 0.5mA
Device under test
+
-
Test all exposed metal surfaces
Also test with plug reversed (Using AC adapter plug as required)
Earth ground

AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.
The use of a substitute replacement component which dose not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

(FOR EUROPEAN MODEL ONLY)

VARO!

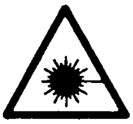
AVATTAESSA JA SUOJALUKITUS OHITETTAESSA OLET ALTTIINA NÄKYMÄTTÖMÄLLE LASERSÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN.

ADVERSEL:

USYNLIG LASERSTRÅLING VED ÅBNING NÅR SIKKERHEDSAFBRYDERE ER UDE AF FUNKTION. UNDGÅ UDSAETTELSE FOR STRÅLING.

VARNING!

OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD OCH SPÄRREN ÄR URKOPPLAD. BETRAKTA EJ STRÅLEN.



LASER
Kuva 1
Lasersateilyn varoitusmerkki

WARNING!

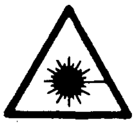
DEVICE INCLUDES LASER DIODE WHICH EMITS INVISIBLE INFRARED RADIATION WHICH IS DANGEROUS TO EYES. THERE IS A WARNING SIGN ACCORDING TO PICTURE 1 INSIDE THE DEVICE CLOSE TO THE LASER DIODE.

IMPORTANT

THIS PIONEER APPARATUS CONTAINS LASER OF CLASS 1.
SERVICING OPERATION OF THE APPARATUS SHOULD BE DONE BY A SPECIALLY INSTRUCTED PERSON.

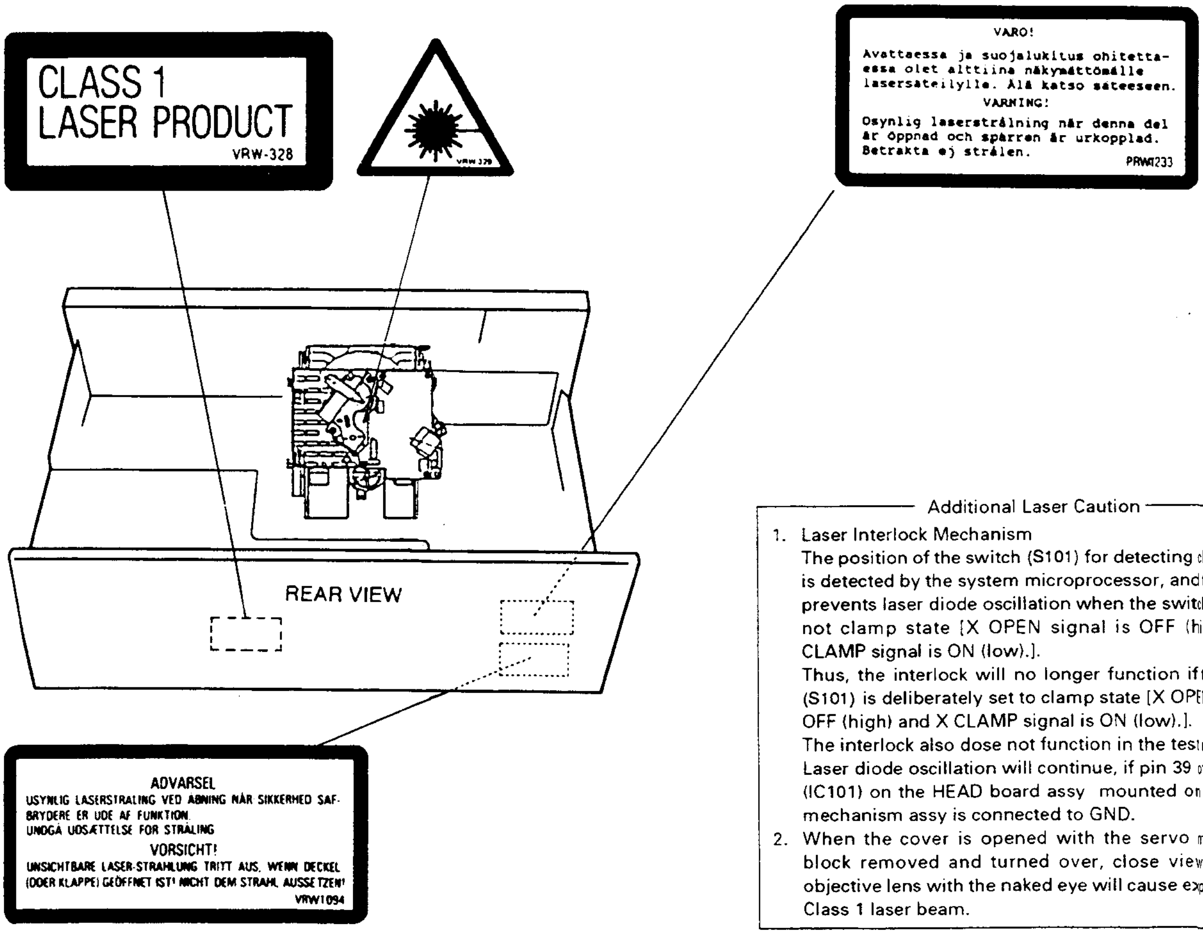
LASER DIODE CHARACTERISTICS

MAXIMUM OUTPUT POWER: 5 mw
WAVELENGTH: 780-785 nm



LASER
Picture 1
Warning sign for laser radiation

LABEL CHECK (PDR-05/ME8 type)



CLASS 1
LASER PRODUCT

VARO!

Avattaessa ja suojalukitus ohitettaessa olet alttiina näkymättömälle lasersäteilylle. Älä katso säteeseen.

VARNING!

Osynlig laserstrålning när denna del är öppnad och spärren är urkopplad. Betrakta ej strålen.

PRW1233

ADVARSEL

USYNLIG LASERSTRALING VED ÅBNING NÅR SIKKERHEDSAFBRYDERE ER UDE AF FUNKTION.
UNDGÅ UDSÆTTELSE FOR STRÅLING

VORSICHT!

UNSICHTBARE LASER-STRAHLUNG TRITT AUS, WENN DECKEL (ODER KLAPPE) GEÖFFNET IST! NICHT DEM STRAHL AUSSETZEN!

VRW1094

Additional Laser Caution

1. Laser Interlock Mechanism
   The position of the switch (S101) for detecting clamp state is detected by the system microprocessor, and the design prevents laser diode oscillation when the switch (S101) is not clamp state [X OPEN signal is OFF (high) and X CLAMP signal is ON (low).].
   Thus, the interlock will no longer function if the switch (S101) is deliberately set to clamp state [X OPEN signal is OFF (high) and X CLAMP signal is ON (low).].
   The interlock also dose not function in the test mode * .
   Laser diode oscillation will continue, if pin 39 of PA4022A (IC101) on the HEAD board assy mounted on the single mechanism assy is connected to GND.
2. When the cover is opened with the servo mechanism block removed and turned over, close viewing of the objective lens with the naked eye will cause exposure to a Class 1 laser beam.

* : Refer to page 49 .

2. PACKING AND PARTS LIST

NOTES:

- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the parts. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by " ⊙ " are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

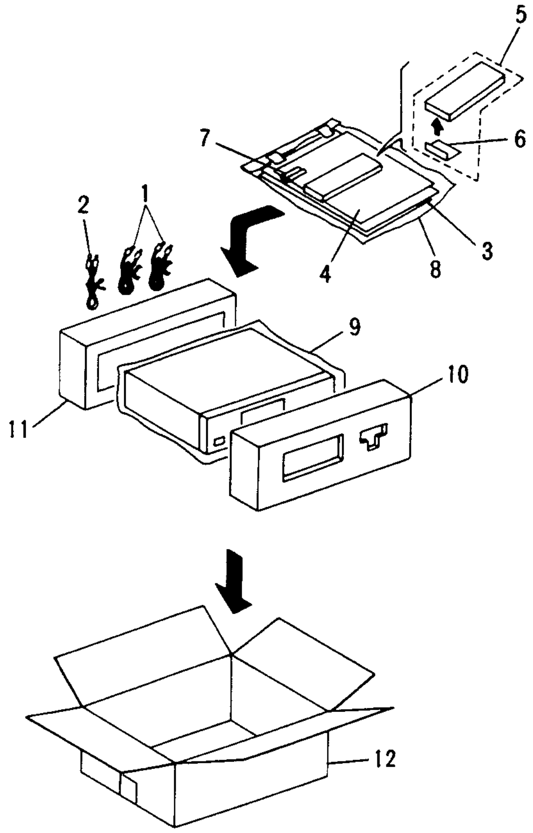
■ CONTRAST OF PDR-99/KU, PDR-05/KU AND PDR-05/ME8

PDR-99/KU, PDR-05/KU and PDR-05/ME8 have the same construction except for the following:

Mark	No.	Symbol & Description	Part No.			Remarks
			PDR-99/KU	PDR-05/KU	PDR-05/ME8	
	2	Cord with mini plug (for SR cord)	PDE1247	PDE1247	Not Used	
	3	Operating instructions (English)	PRB1235	PRB1224	Not used	
	3	Operating instructions (English/French/German/Italian)	Not Used	Not Used	PRE1216	
	3	Operating instructions (Dutch/Swedish/Spanish/Danish)	Not Used	Not Used	PRF1069	
	4	CD-R disc caution card	PRM1046	PRM1046	PRM1045	
	9	Mirror mat	DHL1006	Z23-007	Z23-007	
	10	Styrol protector F	PHA1301	PHA1243	PHA1243	
	11	Styrol protector R	PHA1302	PHA1245	PHA1245	
	12	Packing case	PHG2157	PHG2119	PHG2118	

■ PARTS LIST FOR PDR-99/KU

Mark	No.	Description	Parts No.
	1	Cord with plug	PDE1109
	2	Cord with mini Plug (for SR cord)	PDE1247
	3	Operating instructions (English)	PRB1235
	4	CD-R disc caution card	PRM1046
	5	Wireless remote control unit (CU-PD075)	PWW1103
	6	Battery cover	PZN1010
NSP	7	Battery (R03, AAA)	VEM-022
	8	Polyethylene bag	Z21-038
	9	Mirror mat	DHL1006
	10	Styrol protector F	PHA1301
	11	Styrol protector R	PHA1302
	12	Packing case	PHG2157



3. EXPLODED VIEWS AND PARTS LIST

NOTES:

- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the parts. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by " ⊙ " are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

3.1 EXTERIOR

■ CONTRAST OF PDR-99/KU, PDR-05/KU AND PDR-05/ME8

PDR-99/KU, PDR-05/KU and PDR-05/ME8 have the same construction except for the following:

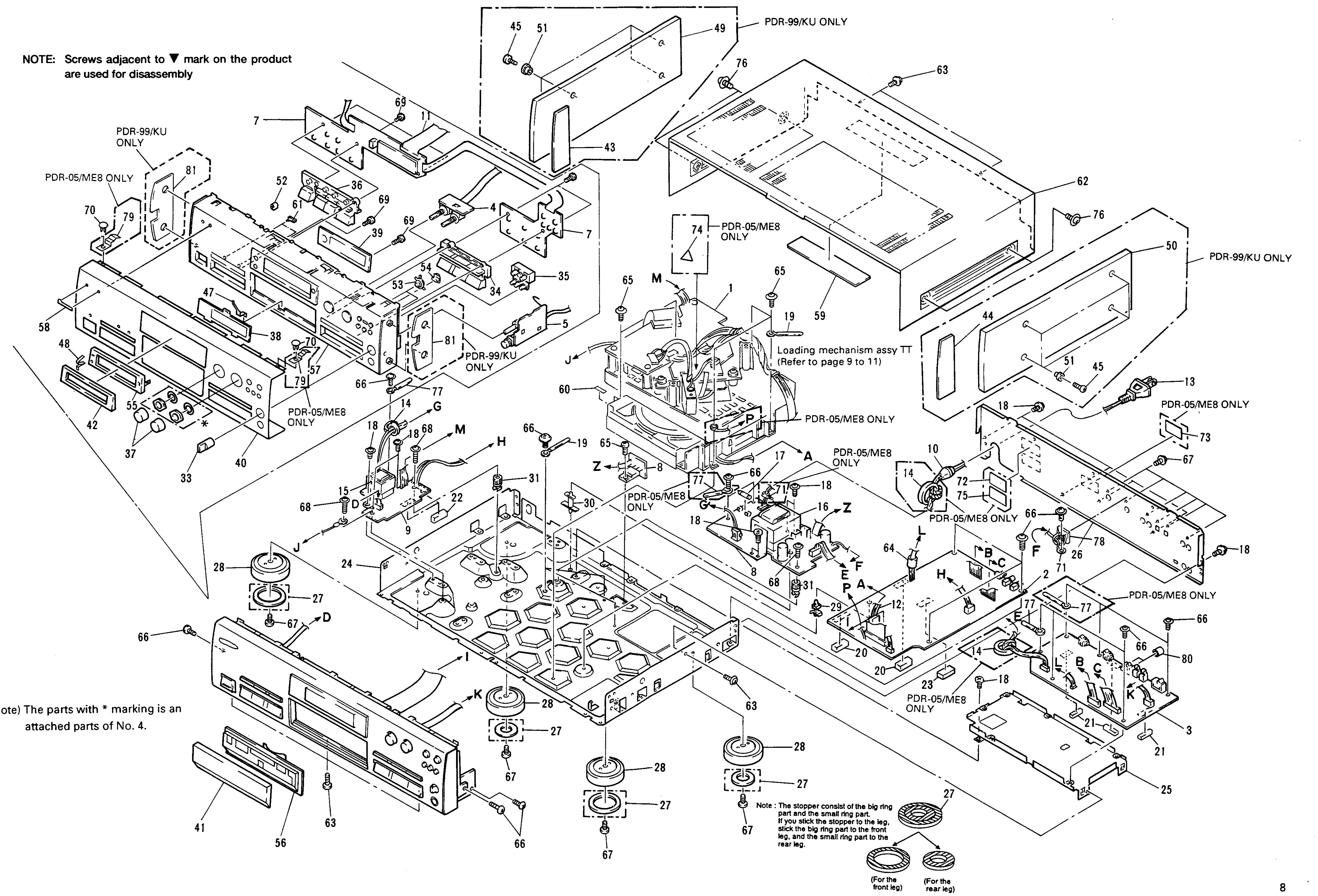
Mark	No.	Symbol & Description	Part No.			Remarks
			PDR-99/KU	PDR-05/KU	PDR-05/ME8	
	2	Servo Ucom board assy	PWZ3027	PWZ3029	PWZ3028	
	3	Audio digital board assy	PWZ3033	PWZ3031	PWZ3032	
	8	Power A board assy	PWZ3049	PWZ3047	PWZ3048	
	9	Power B board assy	PWZ3053	PWZ3051	PWZ3052	
⚠	10	Strain relief	CM-22C	CM-22C	CM-22B	
⚠	13	AC power cord	PDG1015	PDG1015	PDG1003	
	14	Ferrite core	PTH1018	PTH1018	PTH1021	
⚠	15	Power transformer (Servo, AC120V)	PTT1308	PTT1308	Not Used	
⚠	15	Power transformer (Servo, AC220V – 230V)	Not Used	Not Used	PTT1315	
⚠	16	Power transformer (Audio, AC120V)	PTT1309	PTT1309	Not Used	
⚠	16	Power transformer (Audio, AC220V – 230V)	Not Used	Not Used	PTT1316	
⚠	17	Fuse (FU 11, 1A)	REK1075	REK1075	Not Used	
⚠	17	Fuse (FU 11, T500mA)	Not Used	Not Used	AEK1051	
	26	Rear base R99	PNA2247	Not Used	Not Used	
	26	Rear base	Not Used	PNA2201	PNA2200	
	39	FL sheet	PAM1673	PAM1673	PAM1669	
	40	Front panel 99 (AL)	PAN1335	Not Used	Not Used	
	40	Front panel	Not Used	PAN1334	PAN1337	
	41	Name plate 99 (AL)	PAN1325	Not Used	Not Used	
	41	Name plate	Not Used	PAN1308	PAN1332	
	42	Display panel 99 (AL)	PAN1326	Not Used	Not Used	
	42	Display panel	Not Used	PAN1309	PAN1309	
	43	Side mole (L)	PAN1327	Not Used	Not Used	
	44	Side mole (R)	PAN1328	Not Used	Not Used	
	45	Step screw	PBA1103	Not Used	Not Used	
	46	Plate spring	PBK1061	Not Used	Not Used	
	49	Side wood (L)	PMM1041	Not Used	Not Used	
	50	Side wood (R)	PMM1042	Not Used	Not Used	
	51	Wood coller	PNW1238	Not Used	Not Used	
	57	Control panel 99 (AL)	PNW2630	Not Used	Not Used	
	57	Control panel	Not Used	PNW2571	PNW2571	
	59	65 label	ORW1069	ORW1069	Not Used	
	62	Bonnet	PYY1189	PYY1188	PYY1188	
	72	Caution label (HE)	Not Used	Not Used	PRW1233	
NSP	73	Caution label (F)	Not Used	Not Used	VRW-328	
	74	Caution label (G)	Not Used	Not Used	VRW-329	
	75	Caution label	Not Used	Not Used	VRW1094	
	76	Screw	Not Used	FBT40P080FZK	FBT40P080FZK	
	79	Earth plate	Not Used	Not Used	PBK1090	
	81	Sheet	PNM1293	Not Used	Not Used	

■ PARTS LIST FOR PDR-99/KU

Mark	No.	Description	Parts No.
	1	HEAD BOARD ASSY	PWZ3022
	2	SERVO UCOM BOARD ASSY	PWZ3027
	3	AUDIO DIGITAL BOARD ASSY	PWZ3033
NSP	4	REC VR BOARD ASSY	PWZ3034
NSP	5	H.P BOARD ASSY	PWZ3038
NSP	6	MECHANISM BOARD ASSY	PWZ3062
	7	FUNCTION BOARD ASSY	PWZ3042
	8	POWER A BOARD ASSY	PWZ3049
	9	POWER B BOARD ASSY	PWZ3053
⚠	10	Strain relief	CM-22C
	11	39P F.F.C/30V	PDD1163
	12	Connector assy (5P)	PDE1272
⚠	13	AC power cord	PDG1015
	14	Ferrite core	PTH1018
⚠	15	Power transformer (Servo, AC120V)	PTT1308
⚠	16	Power transformer (Audio, AC120V)	PTT1309
⚠	17	Fuse (FU11, 1A)	REK1075
	18	Screw	ABA1207
	19	Cord clamper	RNH-184
NSP	20	Cushion (3.5)	PEB1110
NSP	21	Spacer A	PEB1228
	22	Rubber spacer A	PEB1280
	23	Rubber spacer B	PEB1281
NSP	24	Under base	PNA2195
	25	Audio angle	PNA2197
	26	Rear base 99	PNA2247
	27	Stopper	PNM1285
	28	Insulator	PNW2020
NSP	29	PCB holder	PNW2100
	30	PCB holder	PNW2562
NSP	31	PCB spacer	PNY-404
NSP	32	Loading mechanism assy TT	PXA1568
	33	Headphone knob	PAC1600
	34	Operate button	PAC1744
	35	REC button	PAC1804
	36	Power button	PAC1805
	37	VR knob	PAC1806
	38	Display window	PAM1668
	39	FL sheet	PAM1673
	40	Front panel 99 (AL)	PAN1335
	41	Name plate 99 (AL)	PAN1325
	42	Display panel 99 (AL)	PAN1326
	43	Side mole (L)	PAN1327
	44	Side mole (R)	PAN1328
	45	Step screw	PBA1103
	46	· · · · · ·	
	47	Earth spring B	PBK1138
	48	Earth spring C	PBK1143
	49	Side wood (L)	PMM1041
	50	Side wood (R)	PMM1042
	51	Wood coller	PNW1238
	52	LED lens	PNW2019
	53	REC ring	PNW2558
	54	REC lens	PNW2559
	55	Holder	PNW2591
	56	Tray holder	PNW2592
	57	Control panel 99 (AL)	PNW2630
	58	Name plate (AL)	VAM1032
	59	65 label	ORW1069
	60	Caution label	PRW1244
	61	Indicator lens	PEA1206
	62	Bonnet	PYY1189
	63	Screw	BBT30P080FCC
	64	Ferrite core	PTH1009
	65	Screw	BBZ30P080FCC
	66	Screw	IBZ30P060FCC
	67	Screw	IBZ30P080FCC
	68	Screw	IBZ30P150FCC
	69	Screw	PPZ30P150FMC
	70	Rivet (plastic)	RBM-003
	71	Binder	ZCA-SKB90BK
	72	· · · · · ·	
	73	· · · · · ·	
	74	· · · · · ·	
	75	· · · · · ·	
	76	· · · · · ·	
	77	Cord clamper	DNF1128
NSP	78	Binder holder	PNW1021
	79	· · · · · ·	
NSP	80	Cap	VEC1810
	81	Sheet	PNM1293

Exterior

NOTE: Screws adjacent to ▼ mark on the product are used for disassembly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PDR-99/KU ONLY
PDR-05/ME8 ONLY
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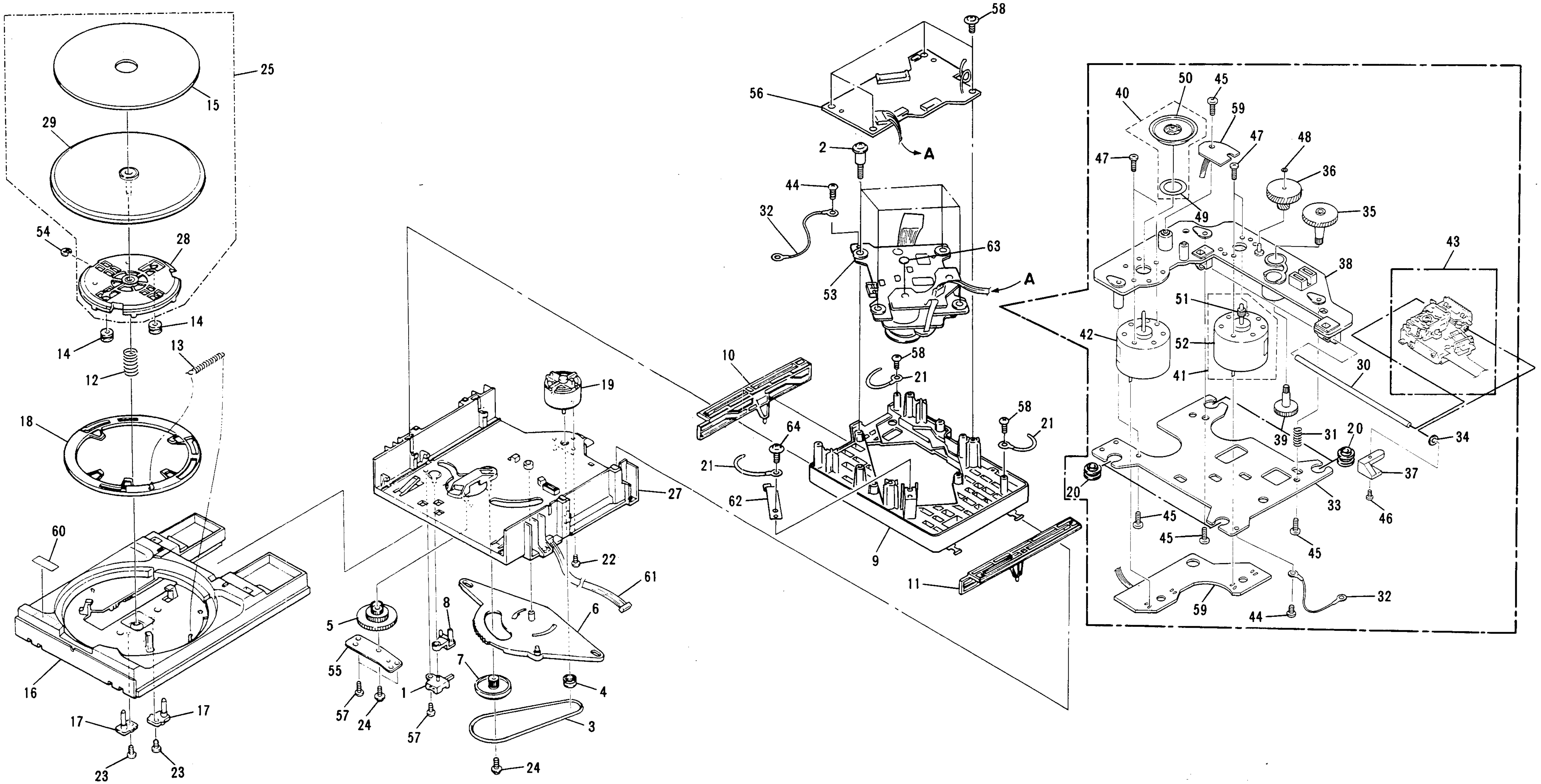
Loading mechanism assy
(Refer to page 9 to 11)
*
(For the front leg)
(For the rear leg)

Note) The parts with * marking is an attached parts of No. 4.

Note : The stopper consist of the big ring part and the small ring part. If you stick the stopper to the leg, stick the big ring part to the front leg, and the small ring part to the rear leg.

3.2 LOADING MECHANISM ASSY TT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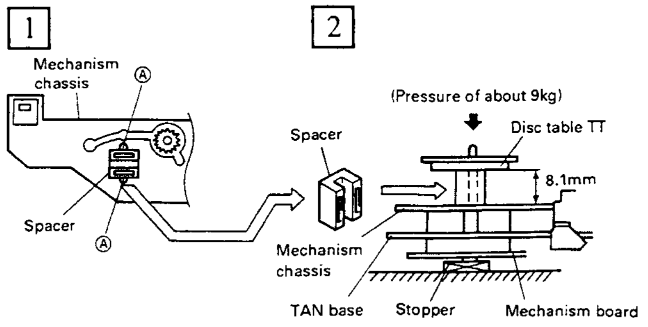
Parts List

Mark	No.	Description	Parts No.
	1	Lever switch (S601)	DSK1003
	2	Float screw	PBA1027
	3	Rubber belt	PEB1186
	4	Motor pulley	PNW1634
	5	Drive gear	PNW1996
	6	Timing lever	PNW2168
	7	Gear pulley	PNW1998
	8	SW head	PNW1999
	9	Float base	PNW2563
	10	Left cam	PNW2001
	11	Right cam	PNW2002
	12	Float spring	PBH1120
	13	Lock spring	PBH1121
	14	Float rubber	PEB1014
	15	Table rubber sheet	PEB1181
	16	Tray	PNW2003
	17	Table guide	PNW2004
	18	Lock plate	PNW2005
	19	D.C. motor (0.75W, LOADING)	PXM1010
	20	Float rubber	PEB1031
	21	Cord clamper	RNH-184
	22	Screw	BMZ26P040FMC
	23	Screw	IPZ26P060FCU
	24	Screw	IPZ20P080FMC
	25	Turn table assy	PEA1165
	26	Screw	IPZ30P080FCU
	27	Loading base	PNW1995
NSP	28	Table shaft holder	PXA1383
NSP	29	Turn table (AL)	PNR1035
	30	Guide shaft	DLA1530
	31	Earth spring	PBH1196
NSP	32	Earth lead unit/300V	PDF1088
	33	TAN base	PNB1514
	34	Stopper ring	PNM1246
	35	Gear 2	PNW2513
	36	Gear 3	PNW2514
	37	TAN plate TT	PNW2518
	38	Mechanism chassis	PNW2520
	39	Gear 1	PNW2521
	40	Disc table TT assy	PEA1323
	41	Carriage moter assy	PEA1324
	42	D.C motor assy (Spindle)	PEA1325
	43	Pickup assy	PEA1326
	44	Screw	BBZ26P040FMC
	45	Screw	BBZ26P080FMC
	46	Screw	BMZ20P040FMC
	47	Screw	JFZ20P030FNI
	48	Washer	WT12D032D025
NSP	49	Mirror mat	PNM1247
NSP	50	Disc table TT	PNW2516
	51	Pinion gear	PNW2515
NSP	52	Spindle D.C motor (0.3W)	PXM1033
NSP	53	SERVO MECHANISM ASSY	PXA1560
	54	Stop ring	YE20S
	55	Shaft holder	PNB1382
	56	HEAD BOARD ASSY	PWZ3022
	57	Screw	BPZ26P060FMC
	58	Screw	IBZ30P080FCC
NSP	59	MECHANISM BOARD ASSY	PWZ3062
	60	Caution label	PRW1244
	61	Connector assy 5P	PDE1243
	62	Clamp spring	PBK1139
	63	Spacer	PBF1014
	64	Screw	IPZ30P080FCC

- How to install the disc table

$\boxed{1}$ Use nippers or other tool to cut the two sections marked Ⓐ in figure $\boxed{1}$. Then remove the spacer.

$\boxed{2}$ While supporting the spindle motor shaft with the stopper, put the spacer on top of the mechanism chassis and stick the disc table TT on top (takes about 9Kg pressure).
Take off the spacer.



4. DISASSEMBLY

4.1 REMOVE THE TRAY PANEL

Hold the tray panel with your hands as shown in Fig. 1, and grasp the tray with your thumbs and then lift the tray panel up while pulling it toward you with the other fingers. (Fig. 2)

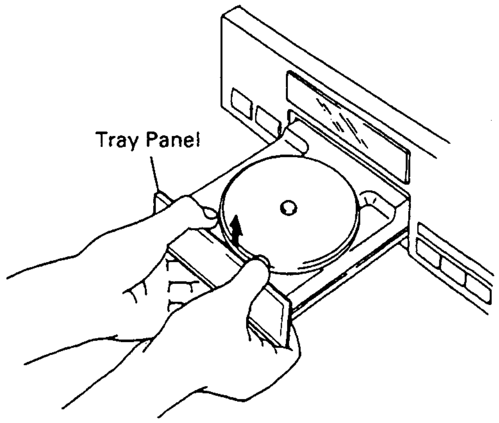


Fig. 1

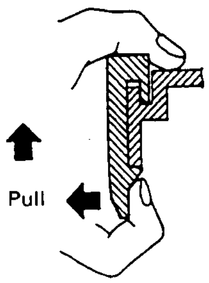


Fig. 2

4.2 INSTALL THE TRAY PANEL

Align the tray panel with the grooves located at both edges of the tray. And then press it down till it stops. (Fig. 3)

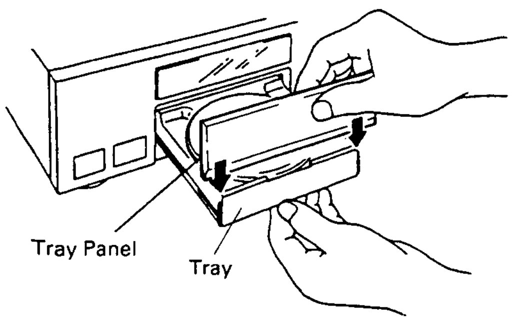

Tray Panel
Tray

Fig. 3

4.3 REMOVE AND SET UP THE HEAD BOARD ASSY

① Remove the bonnet (side wood).
② Remove the tray panel. (Refer to 4.1)
③ Remove the five screws of the front panel.

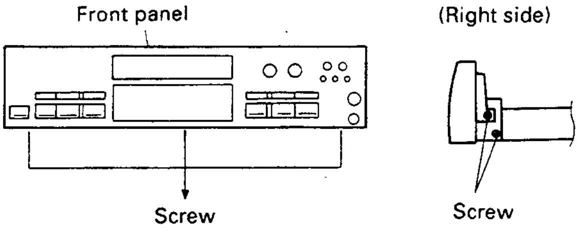

Front panel
(Right side)
Screw
Screw

Fig. 4

④ Pull out the right side of the front panel to the front and remove the four screws of the board.

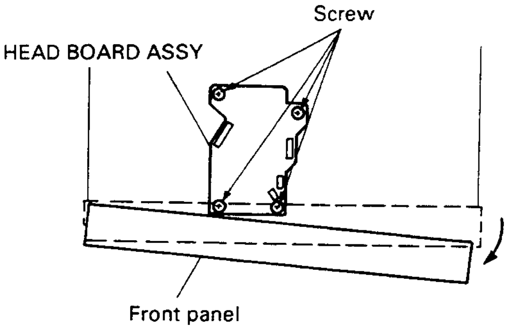

Screw
HEAD BOARD ASSY
Front panel

Fig. 5

⑤ Remove the fixtures of the wires connected to the board (cord holder, PCB binder).
⑥ Place the HEAD BOARD ASSY upright against the slit of the float base.

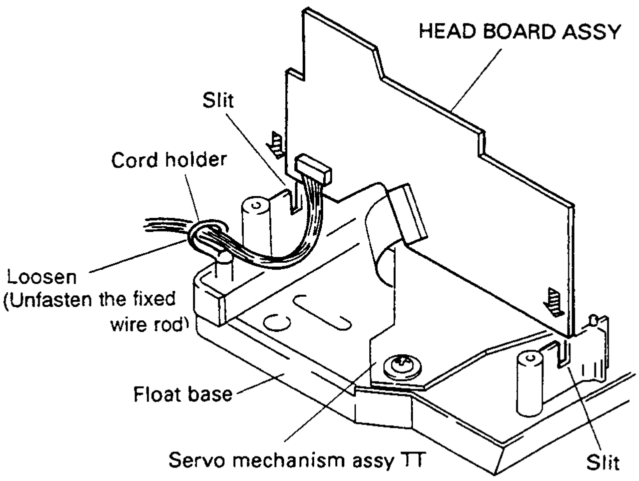
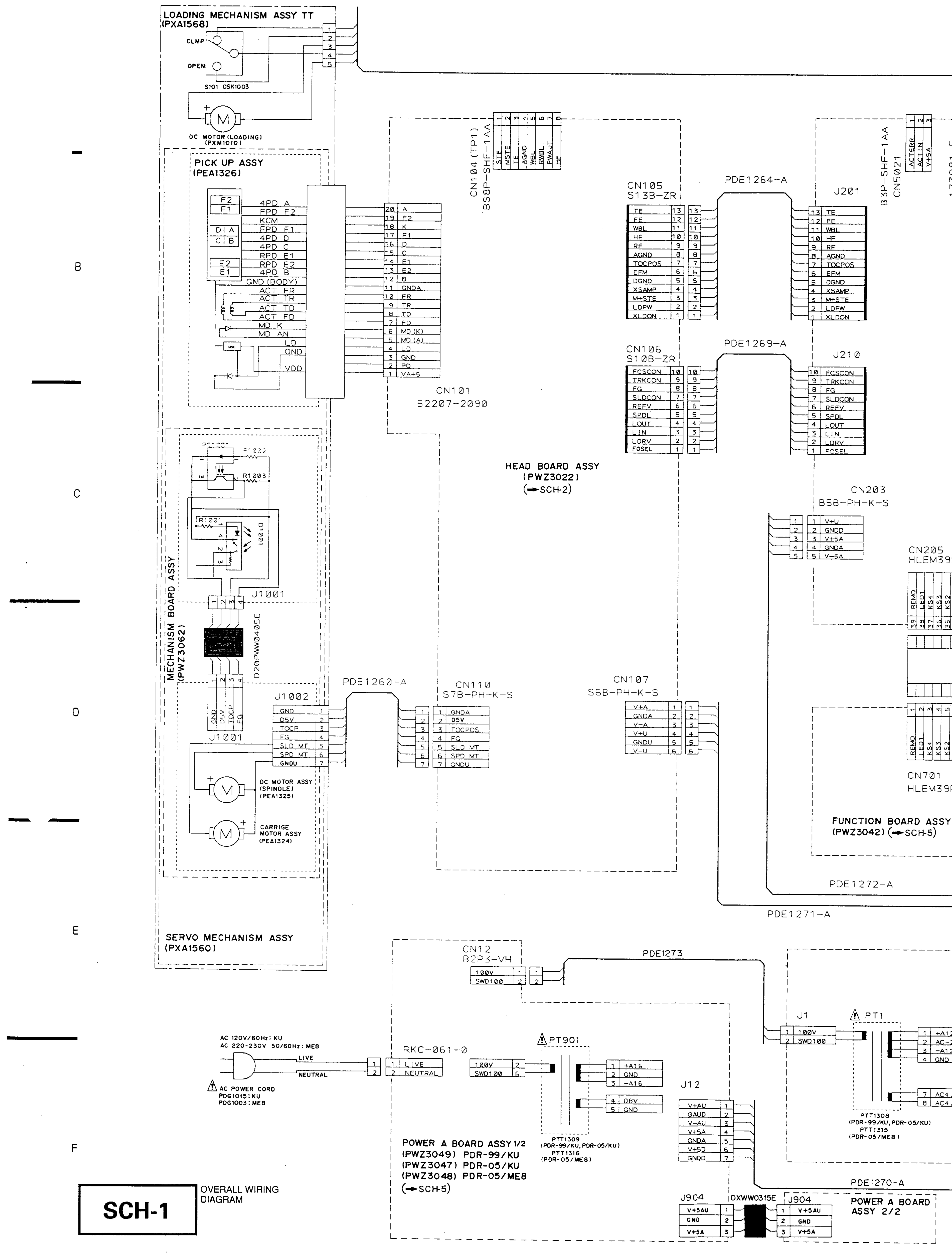

HEAD BOARD ASSY
Slit
Cord holder
Loosen
(Unfasten the fixed wire rod)
Float base
Servo mechanism assy TT
Slit

Fig. 6

5. SCHEMATIC AND PCB CONNECTION DIAGRAMS

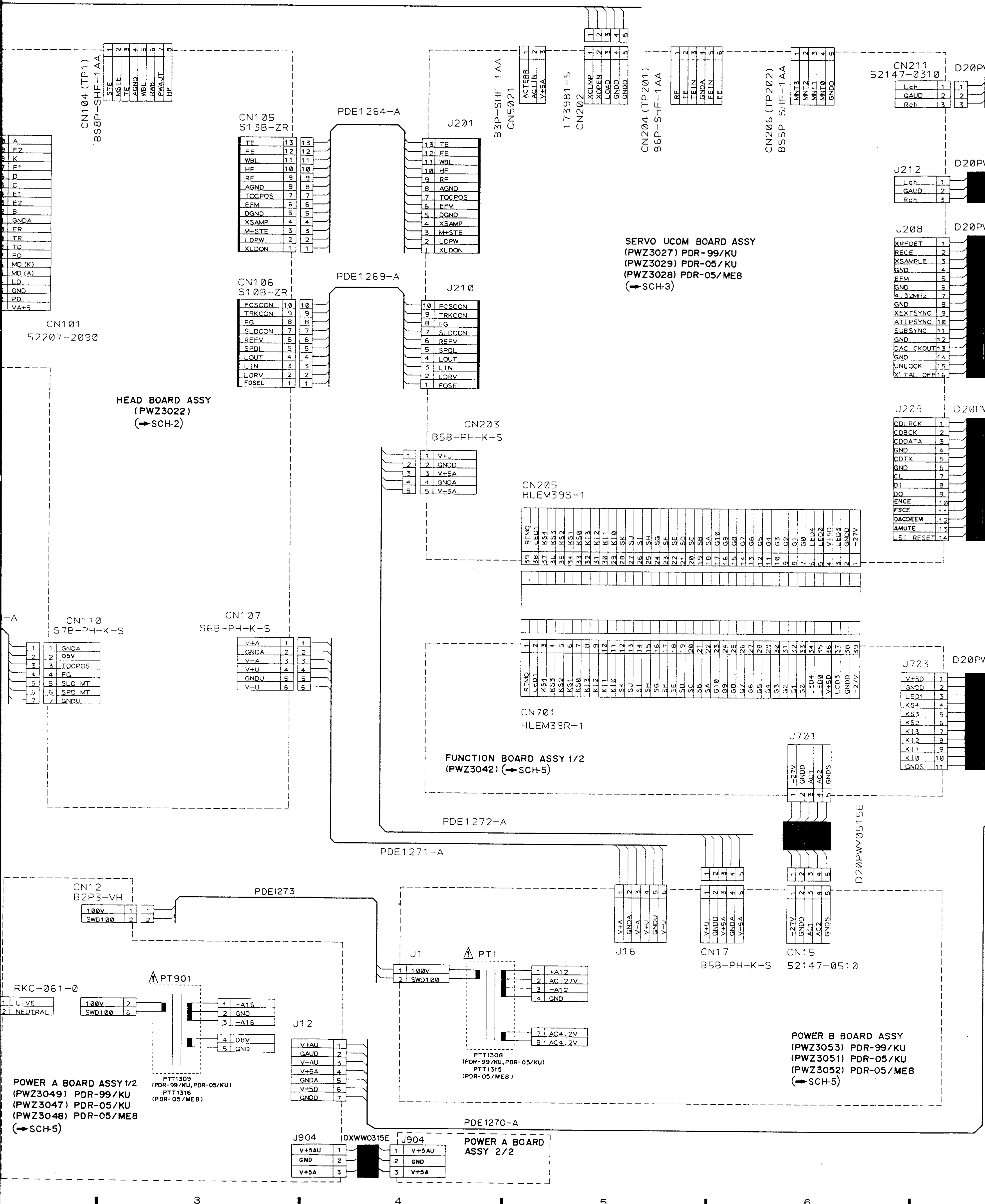
5.1 OVERALL WIRING DIAGRAM

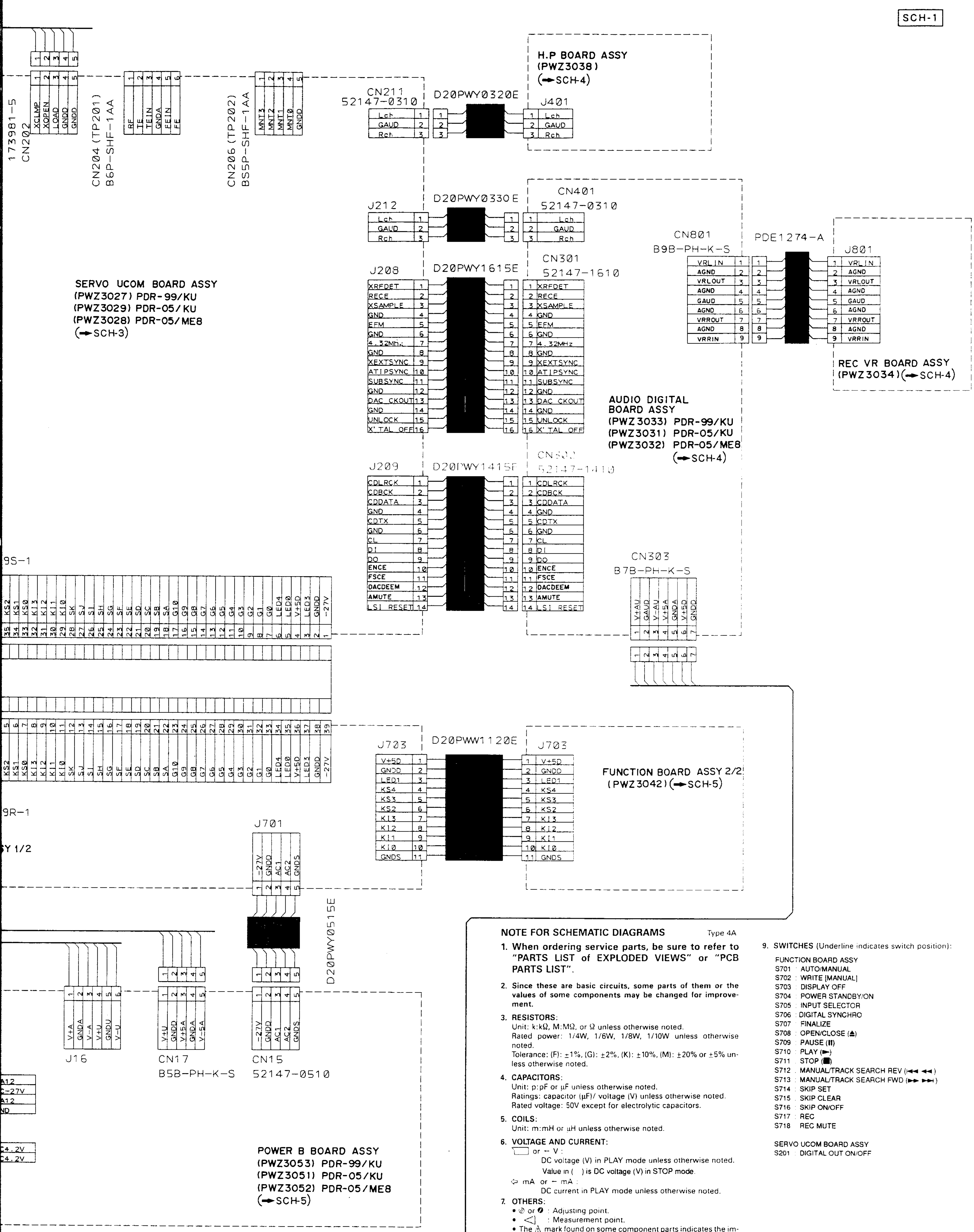

LOADING MECHANISM ASSY TT (PXA1568)
CLMP
OPEN
S101 DSK1003
DC MOTOR (LOADING) (PXM1010)
PICK UP ASSY (PEA1326)
F2
F1
D A
C B
E2
E1
4PD A
FPD F2
KCM
FPD F1
4PD D
4PD C
RPD E1
RPD E2
4PD B
GND (BODY)
ACT FR
ACT TR
ACT TD
ACT FD
MD K
MD AN
LD
GND
VDD
CN104 (TP1) B58P-SHF-1AA
STE
MSTE
TE
AGND
WBL
RWBL
PWAJT
HF
20 A
19 F2
18 K
17 F1
16 D
15 C
14 E1
13 E2
12 B
11 GNDA
10 FR
9 TR
8 TD
7 FD
6 MD (K)
5 MD (A)
4 LD
3 GND
2 PD
1 VA+5
CN101 52207-2090
CN105 S13B-ZR
TE
FE
WBL
HF
RF
AGND
TOCPOS
EFM
DGND
XSAMP
M+STE
LDPW
XLDON
PDE1264-A
J201
B3P-SHF-1AA CN5021
ACTERR
ACTIN
V+5A
CN106 S10B-ZR
FCSCON
TRKCON
FG
SLDCON
REFV
SPDL
LOUT
LIN
LDRV
FOSEL
PDE1269-A
J210
HEAD BOARD ASSY (PWZ3022) (→SCH-2)
CN203 B5B-PH-K-S
V+U
GNDD
V+5A
GNDA
V-5A
CN205 HLEM39
REMO
LED1
KS4
KS3
KS2
CN701 HLEM39
FUNCTION BOARD ASSY (PWZ3042) (→SCH-5)
P1221
R1222
R1003
R1001
D1001
J1001
D20PWW0405E
MECHANISM BOARD ASSY (PWZ3062)
GND
D5V
TOCP
FG
J1002
SLD MT
SPD MT
GNDU
PDE1260-A
CN110 S7B-PH-K-S
GNDA
D5V
TOCPOS
FG
SLD MT
SPD MT
GNDU
CN107 S6B-PH-K-S
V+A
GNDA
V-A
V+U
GNDU
V-U
DC MOTOR ASSY (SPINDLE) (PEA1325)
CARRIGE MOTOR ASSY (PEA1324)
PDE1272-A
PDE1271-A
SERVO MECHANISM ASSY (PXA1560)
CN12 B2P3-VH
100V
SWD100
PDE1273
J1
PT1
100V
SWD100
+A12
AC-
-A12
GND
AC4
PTT1308 (PDR-99/KU, PDR-05/KU)
PTT1315 (PDR-05/ME8)
AC 120V/60Hz: KU
AC 220-230V 50/60Hz: ME8
LIVE
NEUTRAL
AC POWER CORD
PDG1015: KU
PDG1003: ME8
RKC-061-0
LIVE
NEUTRAL
PT901
+A16
GND
-A16
D8V
GND
PTT1309 (PDR-99/KU, PDR-05/KU)
PTT1316 (PDR-05/ME8)
J12
V+AU
GAUD
V-AU
V+5A
GNDA
V+5D
GNDD
PDE1270-A
POWER A BOARD ASSY 1/2
(PWZ3049) PDR-99/KU
(PWZ3047) PDR-05/KU
(PWZ3048) PDR-05/ME8
(→SCH-5)
J904
V+5AU
GND
V+5A
DXWW0315E
POWER A BOARD ASSY 2/2

SCH-1

OVERALL WIRING DIAGRAM

B CONNECTION DIAGRAMS


CN104 (TP1)
BS8P-SHF-1AA
STE
MSTE
TE
AGND
WBL
RWBL
PWAJT
HF
CN105
S13B-ZR
PDE1264-A
J201
TE
FE
WBL
HF
RF
AGND
TOCPOS
EFM
DGND
XSAMP
M+STE
LDPW
XLDON
CN106
S10B-ZR
PDE1269-A
J210
FCSCON
TRKCON
FG
SLDCON
REFV
SPDL
LOUT
LIN
LDRV
FOSEL
A
F2
K
F1
D
C
E1
E2
B
GNDA
FR
TR
TD
FD
MD (K)
MD (A)
LD
GND
PD
VA+5
CN101
52207-2090
HEAD BOARD ASSY
(PWZ3022)
(→SCH-2)
B3P-SHF-1AA
CN5021
ACTERR
ACTIN
V+5A
173981-5
CN202
XCLMP
XOPEN
LOAD
GNDD
GNDD
CN204 (TP201)
B6P-SHF-1AA
RF
TE
TEIN
GNDA
FEIN
FE
CN206 (TP202)
B5SP-SHF-1AA
MNT3
MNT2
MNT1
MNT0
GNDD
CN211
52147-0310
Lch
GAUD
Rch
D20PV
J212
Lch
GAUD
Rch
D20PV
J208
XRFDET
RECE
XSAMPLE
GND
EFM
GND
4.32MHz
GND
XEXTSYNC
ATIPSYNC
SUBSYNC
GND
DAC CKOUT
GND
UNLOCK
X' TAL OFF
D20PV
J209
CDLRCK
CDBCK
CDDATA
GND
CDTX
GND
CL
DI
DO
ENCE
FSCE
DACDEEM
AMUTE
LSI RESET
D20PV
SERVO UCOM BOARD ASSY
(PWZ3027) PDR-99/KU
(PWZ3029) PDR-05/KU
(PWZ3028) PDR-05/ME8
(→SCH-3)
CN203
B5B-PH-K-S
V+U
GNDD
V+5A
GNDA
V-5A
CN205
HLEM39S-1
REMO
LED1
KS4
KS3
KS2
KS1
KS0
KI3
KI2
KI1
KI0
SK
SJ
SH
SG
SF
SE
SD
SC
SB
SA
G10
G9
G8
G7
G6
G5
G4
G3
G2
G1
G0
LED4
LED0
V+5D
LED3
GNDD
-27V
CN701
HLEM39R-1
J703
V+5D
GNDD
LED1
KS4
KS3
KS2
KI3
KI2
KI1
KI0
GNDS
D20PV
J701
-27V
GNDD
AC1
AC2
GNDS
FUNCTION BOARD ASSY 1/2
(PWZ3042) (→SCH-5)
D20PWY0515E
CN110
S7B-PH-K-S
GNDA
D5V
TOCPOS
FG
SLD MT
SPD MT
GNDU
CN107
S6B-PH-K-S
V+A
GNDA
V-A
V+U
GNDU
V-U
PDE1272-A
PDE1271-A
CN12
B2P3-VH
100V
SWD100
PDE1273
J16
V+A
GNDA
V-A
V+U
GNDU
V-U
CN17
B5B-PH-K-S
V+U
GNDD
V+5A
GNDA
V-5A
CN15
52147-0510
-27V
GNDD
AC1
AC2
GNDS
J1
100V
SWD100
⚠ PT1
+A12
AC-27V
-A12
GND
AC4.2V
AC4.2V
PTT1308
(PDR-99/KU, PDR-05/KU)
PTT1315
(PDR-05/ME8)
RKC-061-0
LIVE
NEUTRAL
100V
SWD100
⚠ PT901
+A16
GND
-A16
D8V
GND
PTT1309
(PDR-99/KU, PDR-05/KU)
PTT1316
(PDR-05/ME8)
J12
V+AU
GAUD
V-AU
V+5A
GNDA
V+5D
GNDD
POWER A BOARD ASSY 1/2
(PWZ3049) PDR-99/KU
(PWZ3047) PDR-05/KU
(PWZ3048) PDR-05/ME8
(→SCH-5)
POWER B BOARD ASSY
(PWZ3053) PDR-99/KU
(PWZ3051) PDR-05/KU
(PWZ3052) PDR-05/ME8
(→SCH-5)
PDE1270-A
J904
V+5AU
GND
V+5A
DXWW0315E
J904
V+5AU
GND
V+5A
POWER A BOARD ASSY 2/2


SCH-1
H.P BOARD ASSY (PWZ3038) (→SCH-4)
CN211 52147-0310
D20PWY0320E
J401
Lch
GAUD
Rch
173981-5 CN202
XCLMP
XOPEN
LOAD
GNDD
GNDD
CN204 (TP201) B6P-SHF-1AA
RF
TE
TEIN
GNDA
FEIN
FE
CN206 (TP202) B5SP-SHF-1AA
MNT3
MNT2
MNT1
MNT0
GNDD
J212
D20PWY0330E
CN401 52147-0310
CN801 B9B-PH-K-S
PDE1274-A
J801
VRLIN
AGND
VRLOUT
GAUD
VRROUT
VRRIN
REC VR BOARD ASSY (PWZ3034) (→SCH-4)
J208
D20PWY1615E
CN301 52147-1610
XRFDET
RECE
XSAMPLE
GND
EFM
4.32MHz
XEXTSYNC
ATIPSYNC
SUBSYNC
DAC CKOUT
UNLOCK
X'TAL OFF
SERVO UCOM BOARD ASSY (PWZ3027) PDR-99/KU (PWZ3029) PDR-05/KU (PWZ3028) PDR-05/ME8 (→SCH-3)
AUDIO DIGITAL BOARD ASSY (PWZ3033) PDR-99/KU (PWZ3031) PDR-05/KU (PWZ3032) PDR-05/ME8 (→SCH-4)
J209
D20PWY1415E
CN302 52147-1410
CDLRCK
CDBCK
CDDATA
GND
CDTX
CL
DI
DO
ENCE
FSCE
DACDEEM
AMUTE
LSI RESET
CN303 B7B-PH-K-S
V+AU
GAUD
V-AU
V+5A
GNDA
V+5D
GNDD
9S-1
KS2 KS1 KS0 KI3 KI2 KI1 KI0 SK SJ SI SH SG SF SE SD SC SB SA G10 G9 G8 G7 G6 G5 G4 G3 G2 G1 G0 LED4 LED0 V+5D LED3 GNDD -27V
9R-1
Y 1/2
J703
D20PWW1120E
J703
V+5D
GNDD
LED1
KS4
KS3
KS2
KI3
KI2
KI1
KI0
GNDS
FUNCTION BOARD ASSY 2/2 (PWZ3042) (→SCH-5)
J701
-27V
GNDD
AC1
AC2
GNDS
D20PWY0515E
J16
V+A
GNDA
V-A
V+U
GNDU
V-U
CN17 B5B-PH-K-S
V+U
GNDD
V+5A
GNDA
V-5A
CN15 52147-0510
A12
C-27V
A12
ND
C4.2V
C4.2V
POWER B BOARD ASSY (PWZ3053) PDR-99/KU (PWZ3051) PDR-05/KU (PWZ3052) PDR-05/ME8 (→SCH-5)

NOTE FOR SCHEMATIC DIAGRAMS

Type 4A

1. **When ordering service parts, be sure to refer to "PARTS LIST of EXPLODED VIEWS" or "PCB PARTS LIST".**

2. **Since these are basic circuits, some parts of them or the values of some components may be changed for improvement.**

3. **RESISTORS:**
   Unit: k:kΩ, M:MΩ, or Ω unless otherwise noted.
   Rated power: 1/4W, 1/6W, 1/8W, 1/10W unless otherwise noted.
   Tolerance: (F): ±1%, (G): ±2%, (K): ±10%, (M): ±20% or ±5% unless otherwise noted.

4. **CAPACITORS:**
   Unit: p:pF or μF unless otherwise noted.
   Ratings: capacitor (μF)/ voltage (V) unless otherwise noted.
   Rated voltage: 50V except for electrolytic capacitors.

5. **COILS:**
   Unit: m:mH or μH unless otherwise noted.

6. **VOLTAGE AND CURRENT:**
   ☐ or ← V :
   DC voltage (V) in PLAY mode unless otherwise noted.
   Value in ( ) is DC voltage (V) in STOP mode.
   ⇦ mA or ← mA :
   DC current in PLAY mode unless otherwise noted.

7. **OTHERS:**
   - ⊘ or ● : Adjusting point.
   - ◁ : Measurement point.
   - The ⚠ mark found on some component parts indicates the importance of the safety factor of the parts. Therefore, when replacing, be sure to use parts of identical designation.

8. **SCH−☐ ON THE SCHEMATIC DIAGRAM:**
   - SCH−☐ indicates the drawing number of the schematic diagram. (SCH stands for schematic diagram.)

9. **SWITCHES** (Underline indicates switch position):

FUNCTION BOARD ASSY
S701 : AUTO/MANUAL
S702 : WRITE [MANUAL]
S703 : DISPLAY OFF
S704 : POWER STANDBY/ON
S705 : INPUT SELECTOR
S706 : DIGITAL SYNCHRO
S707 : FINALIZE
S708 : OPEN/CLOSE (▲)
S709 : PAUSE (II)
S710 : PLAY (►)
S711 : STOP (■)
S712 : MANUAL/TRACK SEARCH REV (◄◄◄ ◄◄)
S713 : MANUAL/TRACK SEARCH FWD (►► ►►►)
S714 : SKIP SET
S715 : SKIP CLEAR
S716 : SKIP ON/OFF
S717 : REC
S718 : REC MUTE

SERVO UCOM BOARD ASSY
S201 : DIGITAL OUT ON/OFF

OVERALL WIRING DIAGRAM

SCH-1

Voltages (V) of HEAD BOARD Assy

IC101 (PA4022A) [V]

Pin No.	MODE			Pin No.	MODE		
	STOP	PLAY	REC		STOP	PLAY	REC
1	0.01	—	−0.1	35	0.6	0.6	0.8
2	0.02	−0.12	−0.4	36	0.6	0.6	0.8
3	0	−0.16	0.0	37	1.2	1.2	1.5
4	−4.9	−4.9	−4.9	38	0.1	0.1	3.1
5	0.0	0.0	0.0	39	5.0	0.0	0.0
6	0.0	0.0	0.0	40	0.0	0.0	−0.1
7	0.0	0.0	0.0	41	0.0	0.0	0.0
8	0.0	0.0	0.0	42	0.0	0.0	0.0
9	0.0	0.0	0.0	43	0.0	0.0	0.1
10	0.0	0.0	0.0	44	0.0	−0.1	−0.1
11	0.0	0.0	0.0	45	−4.9	−4.9	−4.9
12	0.0	0.0	0.0	46	0.0	−0.1	−0.1
13	0.0	0.0	0.0	47	0.0	0.0	0.0
14	0.0	0.0	0.0	48	0.0	0.0	0.0
15	0.0	0.0	0.0	49	0.0	0.0	0.0
16	0.0	0.0	—	50	0.0	0.0	0.0
17	0.0	0.0	0.0	51	0.0	0.0	0.0
18	0.0	0.0	0.0	52	0.0	−0.1	0.0
19	0.0	0.0	0.0	53	0.0	−0.1	−0.1
20	0.0	0.0	0.0	54	0.0	0.2	0.2
21	0.0	0.0	0.0	55	0.0	0.0	0.0
22	0.0	0.0	0.0	56	0.0	0.0	0.0
23	1.4	1.4	1.4	57	0.1	0.1	0.1
24	1.4	1.4	1.4	58	−4.0	−4.0	−4.0
25	0.0	0.0	0.9	59	−2.9	−2.7	−2.7
26	0.0	0.2	0.2	60	0.0	0.0	0.0
27	0.0	0.0	1.2	61	0.0	0.0	0.0
28	0.0	0.0	0.0	62	0.0	0.0	0.0
29	5.0	5.0	5.0	63	5.0	5.0	5.0
30	4.2	1.2	1.2	64	−0.1	0.3	0.3
31	−3.4	−1.7	−1.7	65	0.0	−0.1	0.0
32	0.0	0.0	0.0	66	−0.3	1.4	1.2
33	−1.0	0.0	0.0	67	0.0	0.0	0.0
34	4.3	3.6	3.6	68	−0.1	0.0	0.0

IC102 (BA4560F) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0	0.2	1.5
2	1.4	1.4	1.5
3	1.4	1.4	1.4
4	−5.0	−5.0	−5.0
5	0	0	0
6	0	0	0
7	0	0	0.1 to 0.6
8	5	5	5

IC103 (TC7SUSF) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0	0	0
2	0	0	2.0
3	0	–	–
4	0	0	2.0
5	5	–	–

IC104 (BA4560F) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0	−0.1	−0.2
2	0	−0.1	−0.1
3	0	−0.1	−0.1
4	−5.0	—	—
5	0	0	0
6	0	0	0
7	0	0	0
8	5.0	—	—

IC202 (LA6517) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0	0	0
2	9.4	—	—
3	−0.4	−0.4	−0.4
4	−10.0	—	—
5	−0.4	−0.4	−0.4
6	−0.4	−0.4	−0.4
7	0	0.0	0.0
8	0	0.0	0.0

IC203 (LA6520) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.01	0.01	0 to 0.2
2	0.01	0.3	0.1 to 0.4
3	0	0.3	0.2 to 0.3
4	0.04	−0.1	−0.5 to −0.7
5	2.2	2.2	2.2
6	2.2	2.2	2.2
7	0	0	0
8	0	0	0
9	0	0	0
10	—	—	—
11	—	—	—
12	9.4	—	—
	−10.0	—	—

Q101 (2SC2412K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.6	0.6	0.8
C	—	—	—
B	1.2	1.2	1.4

Q102 (2SB1189) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	4.5
C	1.5	1.5	1.8
B	4.3	3.8	3.8

Q103 (2SA1037K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	4.8
C	1.0	1.0	2.2
B	—	—	—

Q104 (2SA1037K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	4.8
C	1.0	1.0	2.2
B	—	—	—

Q105 (2SA1037K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	4.8
C	1.0	1.0	2.2
B	—	—	—

Q106 (2SA1037K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	4.8
C	—	—	—
B	—	—	—

Q107 (2SA1461) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	—	—	—
C	1.5	1.5	1.8
B	3.0	3.0	3.0

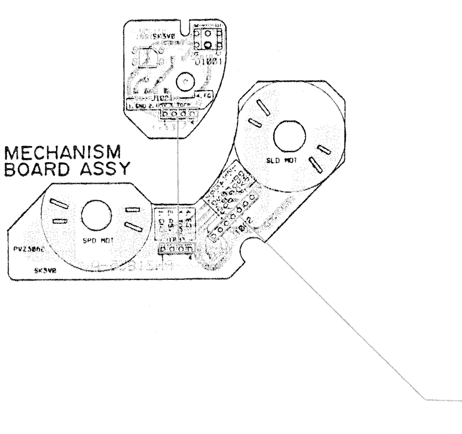
Q109 (DTC114TS) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	—	—
C	0.0	1.1	1.2
B	5.0	0.0	0.0

Q111 (DTA114TK) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	—	—
C	0.0	0.0	4.4
B	5.0	0.0	0.0

- **This diagram is viewed from**
- **This PCB is double sided.**



- The parts mounted on this PCB necessary parts for several destination For further information for respective be sure to check with the schematic di

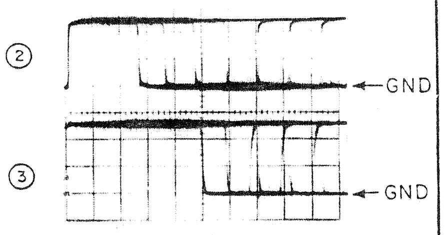
• Waveformes at HEAD BOARD ASSY

• Measuring condition : DC input unless otherwise noted.

② CN105 pin 6 (EFM)

③ CN105 pin 4 (XSAMP)

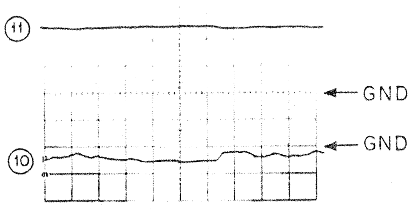
During REC (1kHz 0dB)
2V/div 0.2μS/div



⑪ CN106 pin 5 (SPDL)
1V/div 2ms/div

⑩ IC203 pin 4 (SPD MT)
2V/div 2ms/div

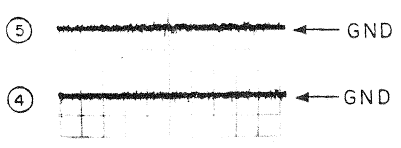
During PLAY



⑤ IC202 pin 6 (FCS ON)

④ IC202 pin 3 (FD)

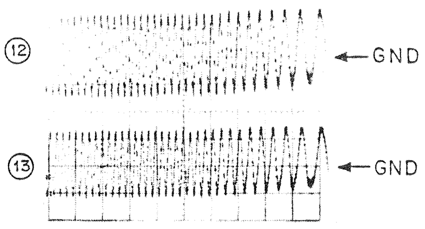
During PLAY
5V/div 1ms/div



⑫ IC101 pin 47 (MTE) 200mV/div

⑬ CN105 pin 3 (M+STE)
500mV/div

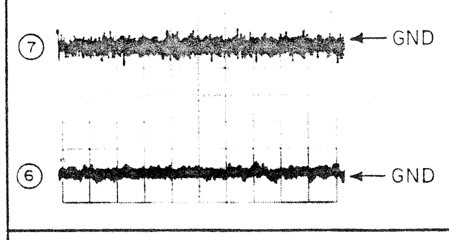
Test mode
CD (FCS SPDL) CLOSE
TRK OPEN



⑦ IC202 pin 7 (TRKC ON)
2V/div 0.5ms/div

⑥ IC202 pin 1 (TD)
0.2V/div 0.5ms/div

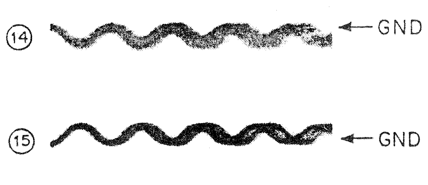
During PLAY



⑭ TP1 pin 5 (WBL)

⑮ CN105 pin 11 (WBL)

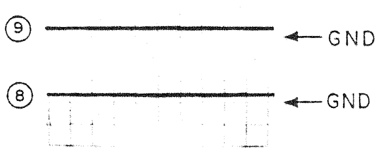
During CD-R PLAY
100mV/div 20μs/div



⑨ IC203 pin 1 (SLDC ON)

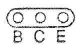
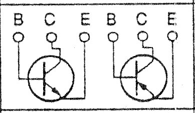
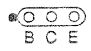
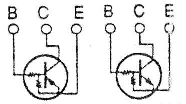
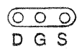
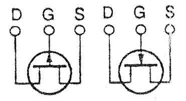
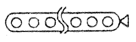
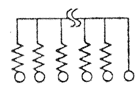
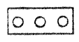
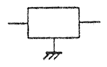
⑧ IC203 pin 3 (SLD MT)

During PLAY
0.5V/div 0.2ms/div

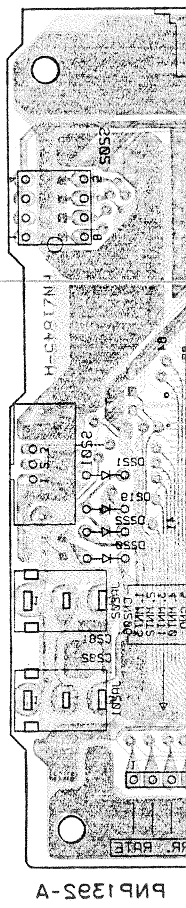


NOTE FOR PCB DIAGRAMS:

1. Part numbers in PCB diagrams match those in the schematic diagrams.
2. A comparison between the main parts of PCB and schematic diagrams is shown below.

Symbol in PCB Diagrams	Symbol in Schematic Diagrams	Part Name
		Transistor
		Transistor with resistor
		Field effect transistor
		Resistor array
		3- terminal regulator

- **This diagram is v**
- **This PCB is doub**



IC202 (LA6517) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0	0	0
2	9.4	—	—
3	− 0.4	− 0.4	− 0.4
4	− 10.0	—	—
5	− 0.4	− 0.4	− 0.4
6	− 0.4	− 0.4	− 0.4
7	0	0.0	0.0
8	0	0.0	0.0

IC203 (LA6520) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.01	0.01	0 to 0.2
2	0.01	0.3	0.1 to 0.4
3	0	0.3	0.2 to 0.3
4	0.04	− 0.1	− 0.5 to − 0.7
5	2.2	2.2	2.2
6	2.2	2.2	2.2
7	0	0	0
8	0	0	0
9	0	0	0
10	—	—	—
11	—	—	—
12	9.4	—	—
	− 10.0	—	—

Q101 (2SC2412K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.6	0.6	0.8
C	—	—	—
B	1.2	1.2	1.4

Q102 (2SB1189) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	4.5
C	1.5	1.5	1.8
B	4.3	3.8	3.8

Q103 (2SA1037K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	4.8
C	1.0	1.0	2.2
B	—	—	—

Q104 (2SA1037K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	4.8
C	1.0	1.0	2.2
B	—	—	—

Q105 (2SA1037K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	4.8
C	1.0	1.0	2.2
B	—	—	—

Q106 (2SA1037K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	4.8
C	—	—	—
B	—	—	—

Q107 (2SA1461) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	—	—	—
C	1.5	1.5	1.8
B	3.0	3.0	3.0

Q109 (DTC114TS) [V]

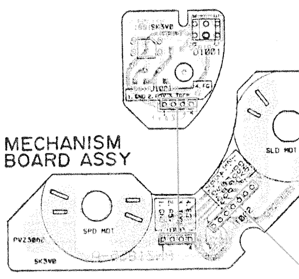
Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	—	—
C	0.0	1.1	1.2
B	5.0	0.0	0.0

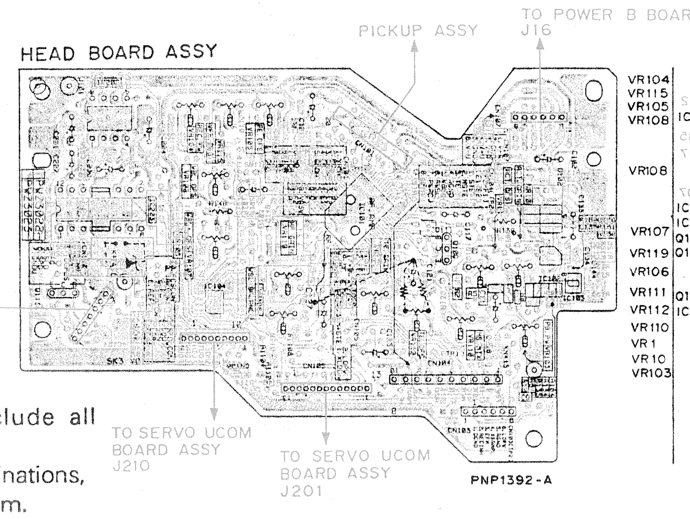
Q111 (DTA114TK) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	—	—
C	0.0	0.0	4.4
B	5.0	0.0	0.0

- This diagram is viewed from the pink colored foil side.
- This PCB is double sided.

PCB-1


MECHANISM BOARD ASSY


HEAD BOARD ASSY
PICKUP ASSY
TO POWER B BOARD ASSY
J16
TO SERVO UCOM BOARD ASSY
J210
TO SERVO UCOM BOARD ASSY
J201
PNP1392-A
VR104
VR115
VR105
VR108
VR108
VR107
VR119
VR106
VR111
VR112
VR110
VR1
VR10
VR103
IC202
IC203
IC101
Q111
Q109
IC102
IC103
Q113
IC104

- The parts mounted on this PCB include all necessary parts for several destinations. For further information for respective destinations, be sure to check with the schematic diagram.

NOTE FOR PCB DIAGRAMS:

1. Part numbers in PCB diagrams match those in the schematic diagrams.
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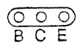
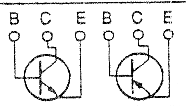
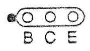
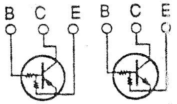
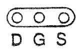
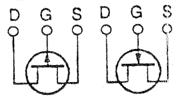
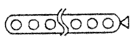
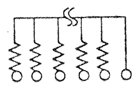
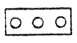
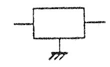
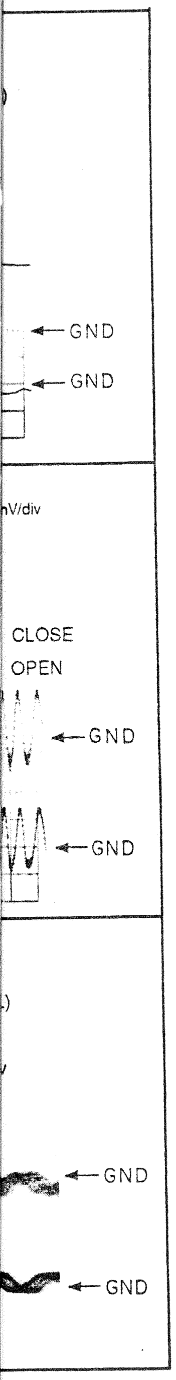
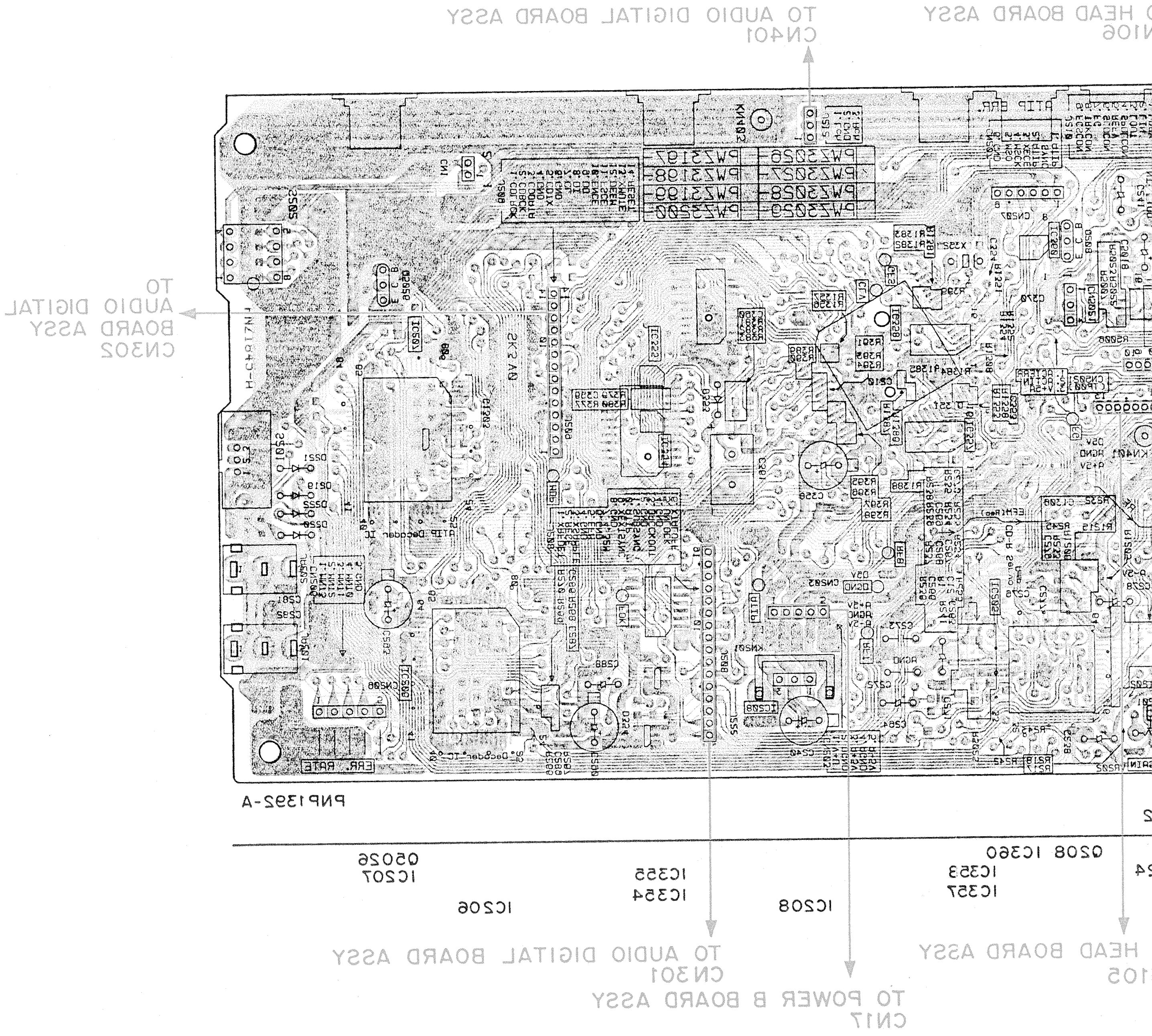
Symbol in PCB Diagrams	Symbol in Schematic Diagrams	Part Name
		Transistor
		Transistor with resistor
		Field effect transistor
		Resistor array
		3- terminal regulator



- This diagram is viewed from the gray colored foil side.
- This PCB is double sided.

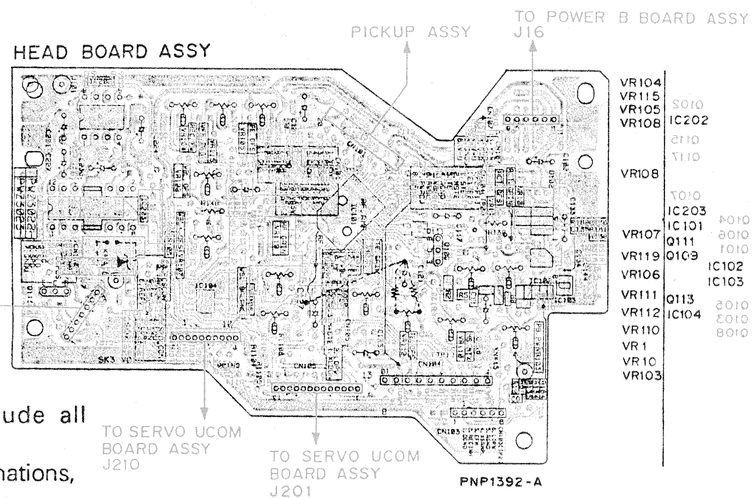
PCB-2


TO AUDIO DIGITAL BOARD ASSY
CN401
HEAD BOARD ASSY
N106
TO
AUDIO DIGITAL
BOARD
ASSY
CN302
PNP1392-A
Q5026
IC207
IC206
IC355
IC354
IC208
Q208 IC360
IC353
IC357
TO AUDIO DIGITAL BOARD ASSY
CN301
TO POWER B BOARD ASSY
CN17
HEAD BOARD ASSY
105

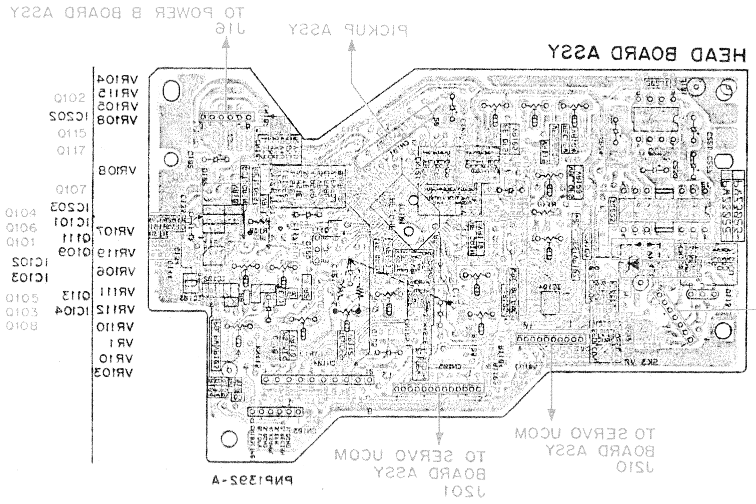
from the pink colored foil side.
ed.

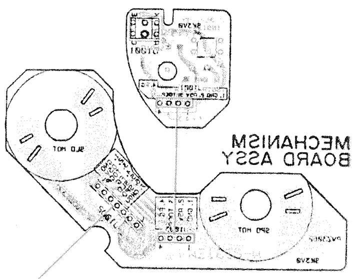
- This diagram is viewed from the gray colored foil side.
- This PCB is double sided.

PCB-1


HEAD BOARD ASSY
PICKUP ASSY
TO POWER B BOARD ASSY J16
VR104
VR115
VR105 IC202
VR108
VR108
IC203
IC101
VR107 Q111
VR119 Q109
VR106 IC102
IC103
VR111 Q113
VR112 IC104
VR110
VR1
VR10
VR103
TO SERVO UCOM BOARD ASSY J210
TO SERVO UCOM BOARD ASSY J201
PNP1392-A

PCB-1

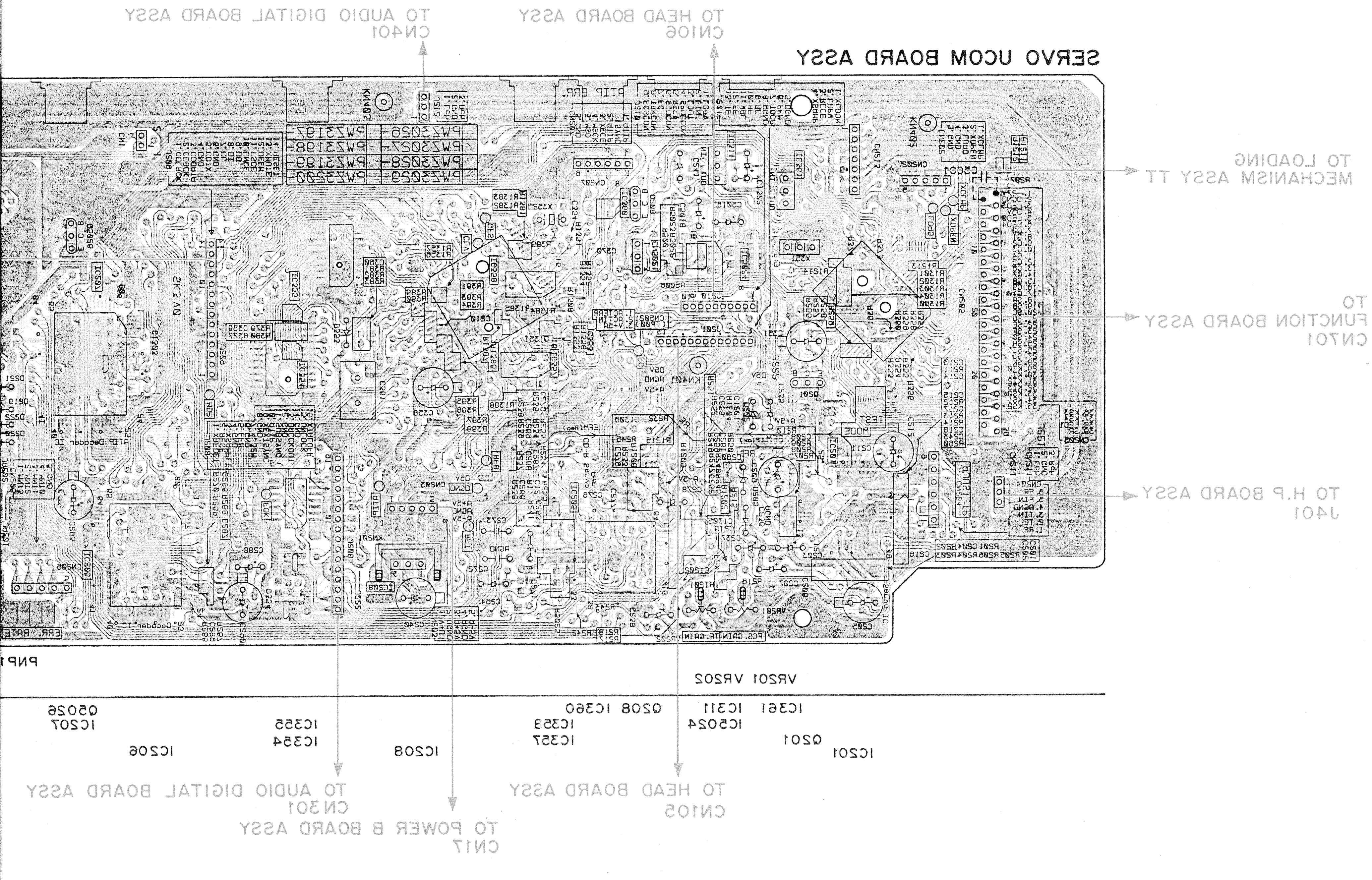

HEAD BOARD ASSY
PICKUP ASSY
TO POWER B BOARD ASSY J16
TO SERVO UCOM BOARD ASSY J201
TO SERVO UCOM BOARD ASSY J210
PNP1392-A


MECHANISM BOARD ASSY

s PCB include all
tinations.
pective destinations,
natic diagram.

m is viewed from the gray colored foil side.
s double sided.

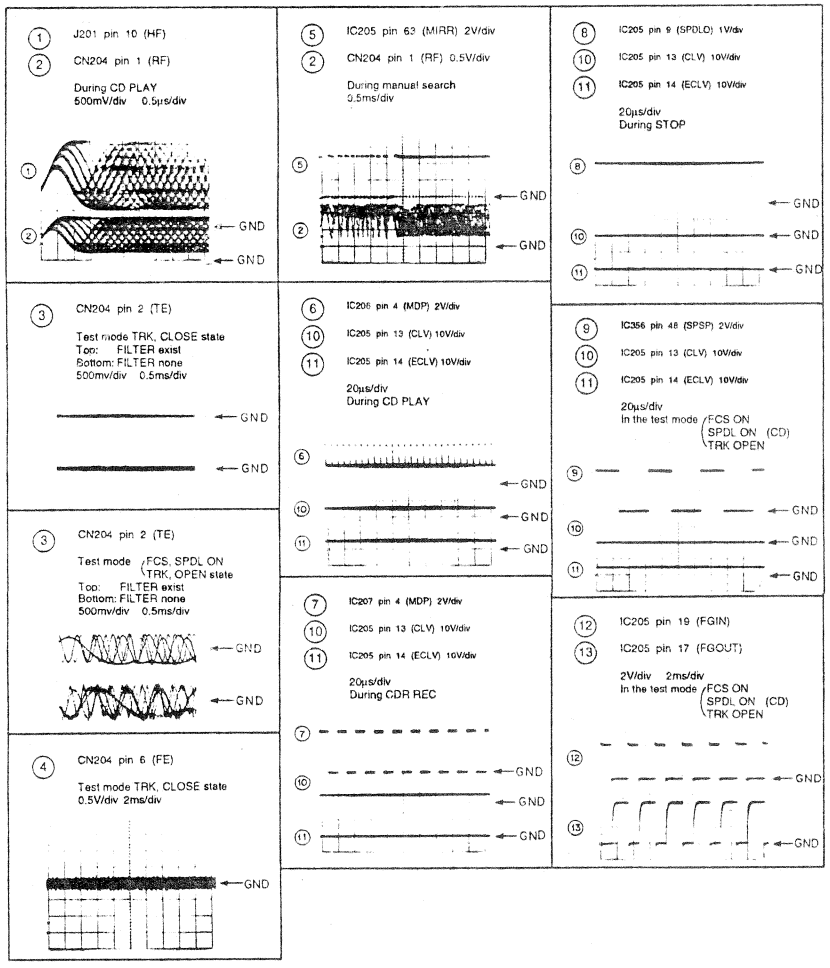
PCB

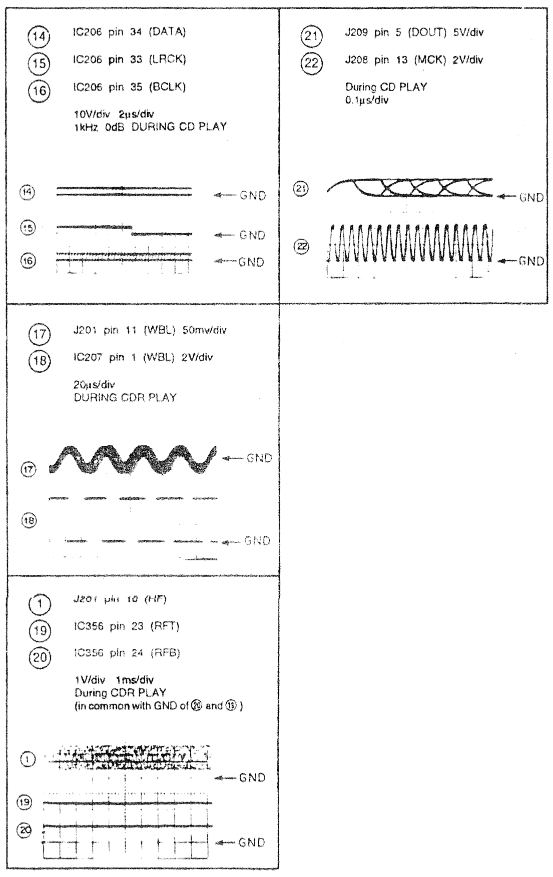

TO AUDIO DIGITAL BOARD ASSY CN401
TO HEAD BOARD ASSY CN106
SERVO UCOM BOARD ASSY
TO LOADING MECHANISM ASSY TT
TO FUNCTION BOARD ASSY CN701
TO H.P BOARD ASSY J401
VR201 VR202
Q5026 IC207
IC206
IC355 IC354
IC208
IC353 IC357
Q208 IC360
IC311 IC5024
IC361
Q201
IC201
TO AUDIO DIGITAL BOARD ASSY CN301
TO POWER B BOARD ASSY CN17
TO HEAD BOARD ASSY CN105

5.3 SERVO UCOM BOARD ASSY

● Waveformes at SERVO UCOM BOARD ASSY

- Measuring condition : DC input unless otherwise noted.





Voltages (V) of SERV

IC201 (CXA1372Q) [V]

Pin No.	MODE			Pin No.
	STOP	PLAY	REC	
1	0.0	0.0	0.0	25
2	0.0	0.0	0.0	26
3	0.0	0.0	0.0	27
4	0.0	0.0	0.0	28
5	−0.4	−0.4	−0.4	29
6	0.0	0.0	0.0	30
7	0.3	0.3	0.3	31
8	0.0	0.0	0.0	32
9	0.0	0.0	0.0	33
10	5.0	5.0	5.0	34
11	0.0	0.0	0.0	35
12	0.0	0.0	0.0	36
13	0.0	0.0	0.0	37
14	0.0	0.3	0.3	38
15	0.0	0.0	0.0	39
16	−4.0	−4.0	−4.0	40
17	1.3	1.3	1.3	41
18	0.0	0.0	0.0	42
19	−4.9	−4.9	−4.9	43
20	5.0	5.0	5.0	44
21	5.0	5.0	5.0	45
22	4.8	4.9	5.0	46
23	5.0	5.0	5.0	47
24	0.7	0.7	0.7	48

● This diagram is viewed from the pink colored foil side.

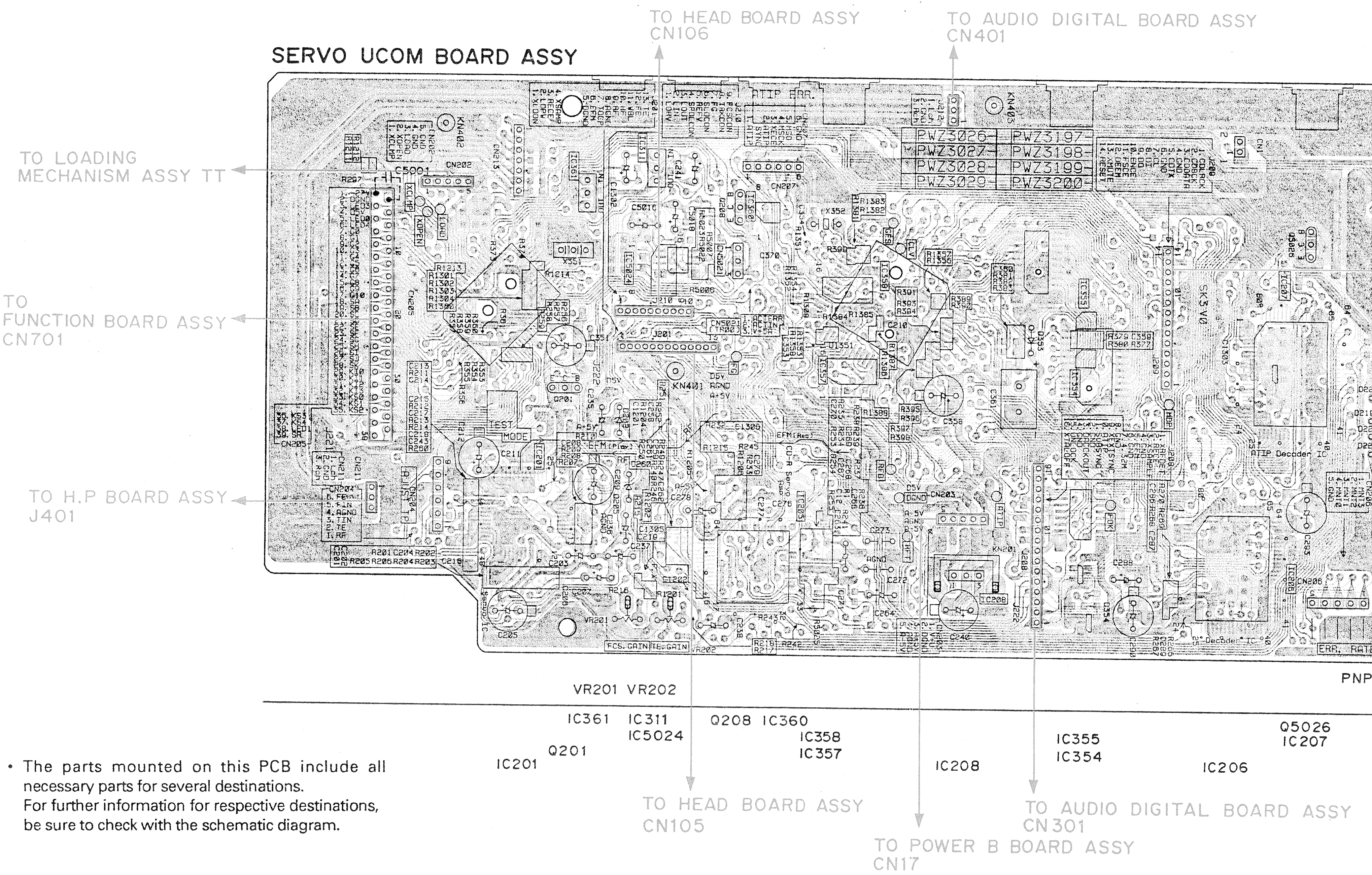
● This PCB is double sided.

Note:

＊1: Ask PIONNER subsidiaries/distributors if these parts are to be replaced or repaired.

PC

SERVO UCOM BOARD ASSY


TO HEAD BOARD ASSY CN106
TO AUDIO DIGITAL BOARD ASSY CN401
TO LOADING MECHANISM ASSY TT
TO FUNCTION BOARD ASSY CN701
TO H.P BOARD ASSY J401
PWZ3026
PWZ3027
PWZ3028
PWZ3029
PWZ3197
PWZ3198
PWZ3199
PWZ3200
TEST MODE
FCS. GAIN
TE. GAIN
ATIP Decoder IC
Decoder IC
Servo IC
ERR. RATE
PNP
VR201 VR202
IC361
IC311
IC5024
Q208 IC360
IC358
IC357
Q201
IC201
IC208
IC355
IC354
IC206
Q5026
IC207
TO HEAD BOARD ASSY CN105
TO AUDIO DIGITAL BOARD ASSY CN301
TO POWER B BOARD ASSY CN17

- The parts mounted on this PCB include all necessary parts for several destinations. For further information for respective destinations, be sure to check with the schematic diagram.

Voltages (V) of SERVO UCOM BOARD Assy

IC201 (CXA1372Q) [V]

Pin No.	MODE			Pin No.	MODE		
	STOP	PLAY	REC		STOP	PLAY	REC
1	0.0	0.0	0.0	25	4.9	4.9	0.0
2	0.0	0.0	0.0	26	0.1	0.1	1.2
3	0.0	0.0	0.0	27	0.8	1.5	1.9
4	0.0	0.0	0.0	28	0.0	0.0	0.0
5	−0.4	−0.4	−0.4	29	0.0	0.0	3.7
6	0.0	0.0	0.0	30	−4.9	−4.9	−4.9
7	0.3	0.3	0.3	31	2.5	2.5	2.5
8	0.0	0.0	0.0	32	2.6	2.6	2.8
9	0.0	0.0	0.0	33	0.1	5.0	5.0
10	5.0	5.0	5.0	34	1.4	−1.1	−4.8
11	0.0	0.0	0.0	35	−1.0	−1.4	−4.8
12	0.0	0.0	0.0	36	5.0	5.0	5.0
13	0.0	0.0	0.0	37	0.0	−0.4	−4.0
14	0.0	0.3	0.3	38	−4.0	−3.2	−1.9
15	0.0	0.0	0.0	39	0.0	0.0	0.0
16	−4.0	−4.0	−4.0	40	−0.1	0.1	3.9
17	1.3	1.3	1.3	41	−4.9	−4.9	−4.9
18	0.0	0.0	0.0	42	0.0	0.0	0.0
19	−4.9	−4.9	−4.9	43	0.0	0.0	0.0
20	5.0	5.0	5.0	44	0.0	0.0	0.0
21	5.0	5.0	5.0	45	0.0	0.0	0.0
22	4.8	4.9	5.0	46	0.0	0.0	0.0
23	5.0	5.0	5.0	47	0.2	0.0	0.0
24	0.7	0.7	0.7	48	0.2	0.0	0.0

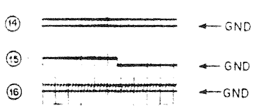
IC205 (PA9004A) [V]

Pin No.	MODE			Pin No.	MODE		
	STOP	PLAY	REC		STOP	PLAY	REC
1	5.0	5.0	5.0	33	3.9	3.9	3.9
2	2.5	2.4	2.5	34	0.0	0.0	0.0
3	3.1	3.1	2.5	35	0.6	0.6	0.6
4	0.8	0.8	2.3	36	0.1	0.1	0.1
5	0.8	0.8	2.3	37	0.0	0.0	0.0
6	2.5	2.5	2.5	38	0.0	0.0	0.0
7	2.5	2.4	1.8	39	0.0	0.0	0.0
8	2.5	2.5	2.5	40	0.0	0.0	0.0
9	2.4	2.6	2.6	41	0.0	0.0	0.0
10	2.5	2.5	2.5	42	0.0	0.0	0.0
11	0.0	0.0	0.0	43	0.0	0.0	0.0
12	2.4	2.4	2.4	44	0.0	0.0	0.0
13	0.0	4.9	4.9	45	5.0	2.4	2.4
14	0.0	4.9	0.0	46	0.0	0.0	0.0
15	2.5	2.5	2.6	47	1.6	0.9	1.2
16	0.0	0.0	0.0	48	1.6	0.9	1.2
17	5.0	2.8	2.8	49	1.6	2.6	1.9
18	−4.0	−4.0	−4.0	50	1.6	2.6	1.9
19	0.0	3.3	3.3	51	1.6	1.6	1.6
20	0.0	0.0	0.0	52	−0.3	1.4	1.8
21	0.0	0.0	0.0	53	−4.0	−4.0	−4.0
22	0.0	0.0	5.0	54	0.3	1.4	2.3
23	0.0	0.0	5.0	55	−1.0	1.5	1.3
24	0.0	0.0	0.0	56	−0.3	1.9	1.9
25	1.0	1.0	1.4	57	0.0	0.0	0.0
26	5.0	5.0	5.0	58	−0.8	−0.6	−0.8
27	0.0	5.0	0.0	59	0.0	0.9	0.3
28	0.0	0.0	0.0	60	0.4	0.4	0.4
29	0.0	0.0	0.0	61	5.0	0.0	5.0
30	0.0	0.0	0.0	62	1.7	0.4	1.7
31	0.0	0.0	0.0	63	5.0	5.0	2.8
32	0.0	0.0	0.0	64	3.9	3.9	3.9

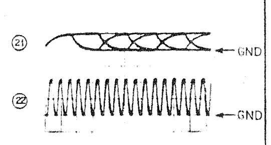
IC206 (CXD2500BQ) [V]

Pin No.	MODE			Pin No.	
	STOP	PLAY	REC		STOP
1	0.1	4.9	4.8	41	1.1
2	0.0	0.2	0.6	42	0.0
3	0.0	5.0	5.0	43	2.5
4	2.4	2.5	3.8	44	5.0
5	0.1	0.2	0.6	45	0.0
6	0.0	5.0	5.0	46	4.3
7	0.1	0.2	0.6	47	3.3
8	5.0	5.0	5.0	48	3.3
9	0.0	0.0	0.0	49	0.0
10	0.0	0.0	0.0	50	1.2
11	0.1	0.2	0.6	51	1.2
12	0.0	0.0	0.0	52	0.0
13	0.1	0.2	0.6	53	2.1
14	0.1	0.2	0.6	54	2.8
15	0.1	0.2	0.3	55	0.0
16	5.0	5.0	5.0	56	2.8
17	0.0	0.0	0.0	57	1.0
18	2.6	2.6	2.6	58	2.1
19	2.5	2.5	2.5	59	5.0
20	2.5	2.5	2.5	60	2.1
21	0.0	0.0	0.0	61	0.0
22	2.6	2.6	2.6	62	2.5
23	5.0	5.0	5.0	63	0.0
24	2.6	2.6	2.8	64	1.5
25	0.0	0.1	0.4	65	0.0
26	0.0	0.0	0.0	66	0.0
27	2.5	2.5	2.5	67	4.9
28	0.0	0.0	0.0	68	0.0
29	0.0	0.1	0.4	69	0.1
30	0.0	0.0	0.0	70	4.9
31	2.5	2.5	2.5	71	0.7
32	0.0	0.1	2.5	72	4.9
33	5.0	5.0	5.0	73	5.0
34	0.0	1.2	0.0	74	4.8
35	1.9	1.9	1.9	75	0.9
36	0.0	1.2	0.0	76	0.8
37	1.9	1.9	1.9	77	0.7
38	2.5	2.5	2.5	78	5.0
39	5.0	0.0	0.0	79	4.8
40	5.0	5.0	5.0	80	0.9

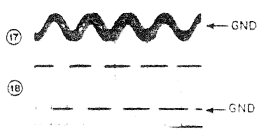
⑭ IC206 pin 34 (DATA)
⑮ IC206 pin 33 (LRCK)
⑯ IC206 pin 35 (BCLK)
10V/div 2μs/div
1kHz 0dB DURING CD PLAY



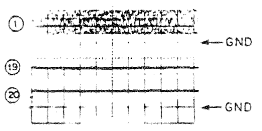
㉑ J209 pin 5 (DOUT) 5V/div
㉒ J208 pin 13 (MCK) 2V/div
During CD PLAY
0.1μs/div



⑰ J201 pin 11 (WBL) 50mv/div
⑱ IC207 pin 1 (WBL) 2V/div
20μs/div
DURING CDR PLAY



① J201 pin 10 (HF)
⑲ IC356 pin 23 (RFT)
⑳ IC356 pin 24 (RFB)
1V/div 1ms/div
During CDR PLAY
(in common with GND of ⑳ and ⑲)

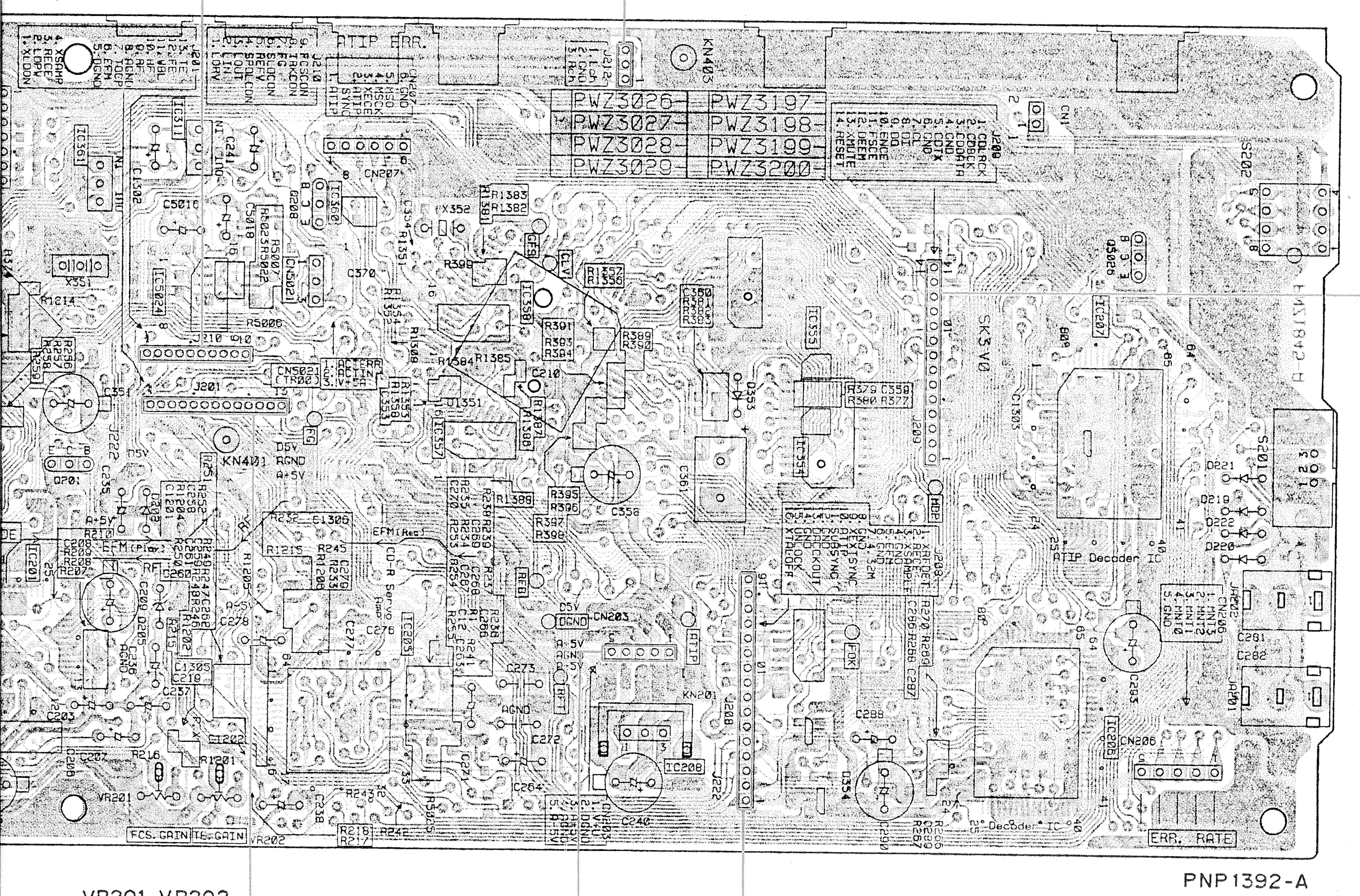


IC351 (PD4591A) [V]

Pin No.	MODE			Pin No.	MODE	
	STOP	PLAY	REC		STOP	PLAY
1	−22.6	−22.0	−22.0	42	4.8	4.8
2	0.0	0.0	0.0	43	0.0	5.0
3	0.0	0.0	0.0	44	0.1	4.9
4	0.0	0.0	−22.0	45	5.0	0.0
5	−22.6	0.0	−22.0	46	0.08	0.0
6	0.0	−22.0	−22.0	47	0.08	0.0
7	−22.6	−22.0	−22.0	48	0.07	0.0
8	5.0	5.0	5.0	49	0.07	0.0
9	0.06	5.0	5.0	50	4.9	4.9
10	0.06	0.0	0 or 5	51	4.9	4.9
11	0.0	0.0	0.0	52	5.0	5.0
12	0.0	0.0	0.0	53	4.7	4.7
13	0.0	0.0	0.0	54	4.7	4.7
14	5.0	0.0	0.0	55	4.7	4.7
15	4.5	0.0	0.0	56	−23.6	−23.2
16	0.8	0.0	0.0	57	−23.6	−23.3
17	5.0	0.0	0.0	58	0.0	0.0
18	5.0	5.0	0.0	59	0.0	0.0
19	0.08	0.0	0.0	60	0.0	0.0
20	0.08	0.0	0.0	61	0.0	0.0
21	0.08	0.0	0.0	62	0.0	0.0
22	0.05	0.0	0.0	63	0.0	0.0
23	0.05	5.0	5.0	64	0.0	5.0
24	0.0	0.0	0.0	65	−24.6	−24.3
25	5.0	5.0	5.0	66	−13.8	−13.6
26	0.06	5.0	—	67	−21.8	−13.4
27	0.06	0.0	0.0	68	−24.5	−24.4
28	0.0	0.0	0.1	69	−24.6	−16.3
29	0.06	0.0	0.1	70	−8.8	−13.3
30	0.06	0.0	0.1	71	−25.0	−24.6
31	0.0	0.0	0.1	72	−12.1	−11.7
32	0.07	0.0	0.1			
33	0.07	0.0	0.1	73	−12.0	(−14.0 to 8.0)
34	0.07	0.0	0.1			
35	0.06	0.0	0.1	74	−9.6	−9.4
36	0.0	0.0	0.1	75	−9.6	−9.4
37	0.06	0.0	0.1	76	−12.1	−6.9
38	0.06	0.0	0.1	77	−22.4	−22.1
39	0.0	0.0	0.1	78	−22.4	−22.1
40	0.05	4.9	4.9	79	−22.3	−22.0
41	4.8	4.8	4.8	80	−22.4	−22.0

PCB-2

ASSY


TO HEAD BOARD ASSY CN106
TO AUDIO DIGITAL BOARD ASSY CN401
TO AUDIO DIGITAL BOARD ASSY CN302
PWZ3026
PWZ3027
PWZ3028
PWZ3029
PWZ3197
PWZ3198
PWZ3199
PWZ3200
ATIP ERR.
ATIP Decoder IC
FCS. GAIN
TE. GAIN
ERR. RATE
PNP1392-A
VR201 VR202
IC361 IC311 IC5024
Q208 IC360
IC358 IC357
Q201
201
IC208
IC355 IC354
Q5026 IC207
IC206
TO HEAD BOARD ASSY CN105
TO POWER B BOARD ASSY CN17
TO AUDIO DIGITAL BOARD ASSY CN301

IC357 (TC74HC367AF) [V]

Pin No.	MODE	
	STOP	PLAY
1	4.4	4.3
2	0.0	0.0
3	0.0	0.0
4	4.5	4.4
5	4.5	2.3
6	5.4	5.0
7	4.7	2.5
8	0.0	0.0
9	4.8	4.8
10	4.8	4.8
11	0.0	0.0
12	0.0	0.0
13	4.8	4.7
14	4.5	4.4
15	4.5	4.4
16	5.0	5.0

IC358 (TC74HC367AF) [V]

Pin No.	MODE	
	STOP	PLAY
1	0.6	0.6
2	4.9	4.9
3	4.8	4.9
4	4.9	4.9
5	4.8	4.8
6	4.3	1.8 to 2.3
7	4.7	2.5
8	0.0	0.0
9	4.4	2.2
10	4.4	2.2
11	4.8	4.7
12	0.0	4.6
13	5.0	4.9
14	4.9	4.8
15	5.0	4.8
16	5.0	5.0

IC359 (TC7S04F) [V]

Pin No.	MODE	
	STOP	PLAY
1	0.0	0.0
2	0.2	0.3
3	0.0	0.0
4	4.7	4.7
5	5.0	5.0

ERVO UCOM BOARD Assy

	Pin No.	MODE		
		STOP	PLAY	REC
0	25	4.9	4.9	0.0
0	26	0.1	0.1	1.2
0	27	0.8	1.5	1.9
0	28	0.0	0.0	0.0
4	29	0.0	0.0	3.7
0	30	−4.9	−4.9	−4.9
3	31	2.5	2.5	2.5
0	32	2.6	2.6	2.8
0	33	0.1	5.0	5.0
0	34	1.4	−1.1	−4.8
0	35	−1.0	−1.4	−4.8
0	36	5.0	5.0	5.0
0	37	0.0	−0.4	−4.0
3	38	−4.0	−3.2	−1.9
0	39	0.0	0.0	0.0
0	40	−0.1	0.1	3.9
3	41	−4.9	−4.9	−4.9
0	42	0.0	0.0	0.0
9	43	0.0	0.0	0.0
0	44	0.0	0.0	0.0
0	45	0.0	0.0	0.0
0	46	0.0	0.0	0.0
0	47	0.2	0.0	0.0
7	48	0.2	0.0	0.0

IC205 (PA9004A) [V]

Pin No.	MODE			Pin No.	MODE		
	STOP	PLAY	REC		STOP	PLAY	REC
1	5.0	5.0	5.0	33	3.9	3.9	3.9
2	2.5	2.4	2.5	34	0.0	0.0	0.0
3	3.1	3.1	2.5	35	0.6	0.6	0.6
4	0.8	0.8	2.3	36	0.1	0.1	0.1
5	0.8	0.8	2.3	37	0.0	0.0	0.0
6	2.5	2.5	2.5	38	0.0	0.0	0.0
7	2.5	2.4	1.8	39	0.0	0.0	0.0
8	2.5	2.5	2.5	40	0.0	0.0	0.0
9	2.4	2.6	2.6	41	0.0	0.0	0.0
10	2.5	2.5	2.5	42	0.0	0.0	0.0
11	0.0	0.0	0.0	43	0.0	0.0	0.0
12	2.4	2.4	2.4	44	0.0	0.0	0.0
13	0.0	4.9	4.9	45	5.0	2.4	2.4
14	0.0	4.9	0.0	46	0.0	0.0	0.0
15	2.5	2.5	2.6	47	1.6	0.9	1.2
16	0.0	0.0	0.0	48	1.6	0.9	1.2
17	5.0	2.8	2.8	49	1.6	2.6	1.9
18	−4.0	−4.0	−4.0	50	1.6	2.6	1.9
19	0.0	3.3	3.3	51	1.6	1.6	1.6
20	0.0	0.0	0.0	52	−0.3	1.4	1.8
21	0.0	0.0	0.0	53	−4.0	−4.0	−4.0
22	0.0	0.0	5.0	54	0.3	1.4	2.3
23	0.0	0.0	5.0	55	−1.0	1.5	1.3
24	0.0	0.0	0.0	56	−0.3	1.9	1.9
25	1.0	1.0	1.4	57	0.0	0.0	0.0
26	5.0	5.0	5.0	58	−0.8	−0.6	−0.8
27	0.0	5.0	0.0	59	0.0	0.9	0.3
28	0.0	0.0	0.0	60	0.4	0.4	0.4
29	0.0	0.0	0.0	61	5.0	0.0	5.0
30	0.0	0.0	0.0	62	1.7	0.4	1.7
31	0.0	0.0	0.0	63	5.0	5.0	2.8
32	0.0	0.0	0.0	64	3.9	3.9	3.9

IC206 (CXD2500BQ) [V]

Pin No.	MODE			Pin No.	MODE		
	STOP	PLAY	REC		STOP	PLAY	REC
1	0.1	4.9	4.8	41	1.1	1.1	1.1
2	0.0	0.2	0.6	42	0.0	5.0	5.0
3	0.0	5.0	5.0	43	2.5	2.5	2.5
4	2.4	2.5	3.8	44	5.0	0.0	0.0
5	0.1	0.2	0.6	45	0.0	5.0	5.0
6	0.0	5.0	5.0	46	4.3	4.4	4.4
7	0.1	0.2	0.6	47	3.3	0.0	0.0
8	5.0	5.0	5.0	48	3.3	0.0	0.0
9	0.0	0.0	0.0	49	0.0	0.0	0.0
10	0.0	0.0	0.0	50	1.2	1.2	1.2
11	0.1	0.2	0.6	51	1.2	1.2	1.2
12	0.0	0.0	0.0	52	0.0	0.0	0.0
13	0.1	0.2	0.6	53	2.1	2.1	2.1
14	0.1	0.2	0.6	54	2.8	2.7	2.7
15	0.1	0.2	0.3	55	0.0	0.0	0.0
16	5.0	5.0	5.0	56	2.8	2.7	2.7
17	0.0	0.0	0.0	57	1.0	1.0	1.0
18	2.6	2.6	2.6	58	2.1	2.1	2.1
19	2.5	2.5	2.5	59	5.0	5.0	5.0
20	2.5	2.5	2.5	60	2.1	2.1	2.1
21	0.0	0.0	0.0	61	0.0	0.0	0.0
22	2.6	2.6	2.6	62	2.5	2.5	2.5
23	5.0	5.0	5.0	63	0.0	0.1	0.1
24	2.6	2.6	2.8	64	1.5	0.1	0.1
25	0.0	0.1	0.4	65	0.0	0.0	0.0
26	0.0	0.0	0.0	66	0.0	4.6	4.7
27	2.5	2.5	2.5	67	4.9	4.9	4.9
28	0.0	0.0	0.0	68	0.0	0.0	0.0
29	0.0	0.1	0.4	69	0.1	2.7	2.8
30	0.0	0.0	0.0	70	4.9	4.9	4.9
31	2.5	2.5	2.5	71	0.7	0.6	0.7
32	0.0	0.1	2.5	72	4.9	4.9	4.9
33	5.0	5.0	5.0	73	5.0	5.0	5.0
34	0.0	1.2	0.0	74	4.8	4.9	4.9
35	1.9	1.9	1.9	75	0.9	1.4	1.7
36	0.0	1.2	0.0	76	0.8	0.1	1.7
37	1.9	1.9	1.9	77	0.7	0.6	0.7
38	2.5	2.5	2.5	78	5.0	5.0	5.0
39	5.0	0.0	0.0	79	4.8	4.9	4.9
40	5.0	5.0	5.0	80	0.9	0.1	1.8

IC207 (PDJ006A) [V]

Pin No.	MODE			Pin No.	MODE		
	STOP	PLAY	REC		STOP	PLAY	REC
1	0.1	2.3	2.1	41	4.9	5.0	4.9
2	5.0	0.0	2.8	42	5.0	5.0	5.0
3	0.1	0.0	0.1	43	5.0	5.0	5.0
4	5.0	5.0	2.5	44	5.0	5.0	5.0
5	0.0	0.0	0.0	45	0.0	0.0	0.0
6	0.3	0.0	0.2	46	0.0	0.0	0.0
7	0.0	0.0	0.0	47	0.0	0.0	0.0
8	0.0	0.0	0.0	48	0.0	0.0	0.0
9	5.0	5.0	5.0	49	0.0	0.0	0.0
10	0.1	0.1	0.2	50	0.0	0.0	0.0
11	5.0	5.0	5.0	51	0.0	0.0	0.0
12	5.0	5.0	5.0	52	0.0	0.0	0.0
13	2.4	0.0	2.4	53	0.0	0.0	0.0
14	4.9	4.9	4.9	54	0.0	0.0	0.0
15	0.0	0.0	5.0	55	0.0	0.0	0.0
16	0.0	0.0	5.0	56	0.0	0.0	0.0
17	0.0	5.0	5.0	57	0.0	0.0	0.0
18	5.0	5.0	5.0	58	5.0	5.0	5.0
19	0.1	0.1	0.4	59	1.9	1.6	2.5
20	4.9	4.9	—	60	5.0	5.0	5.0
21	4.9	4.9	4.9	61	0.0	0.0	0.0
22	4.9	4.9	4.9	62	0.0	0.0	0.0
23	1.6	0.9	1.3	63	0.0	5.0	5.0
24	3.3	2.4	2.2	64	0.0	5.0	0.0
25	3.6	3.3	2.2	65	5.0	0.0	0.0
26	4.1	3.2	3.5	66	5.0	5.0	5.0
27	1.1	0.9	1.1	67	5.0	5.0	5.0
28	0.0	0.0	0.0	68	0.0	0.0	0.0
29	1.4	1.0	1.7	69	5.0	0.0	5.0
30	0.5	0.7	0.8	70	5.0	0.0	0.0
31	4.7	4.7	4.7	71	0.0	5.0	5.0
32	2.8	3.4	3.1	72	0.0	0.0	0.0
33	3.0	3.1	3.3	73	0.0	0.0	0.0
34	3.2	3.2	2.8	74	0.0	0.0	0.0
35	3.2	3.4	2.9	75	0.0	0.0	0.0
36	1.8	1.8	2.5	76	0.0	0.0	0.0
37	3.4	3.2	3.4	77	0.0	0.0	0.0
38	5.0	5.0	5.0	78	5.0	5.0	5.0
39	1.2	1.4	1.3	79	0.0	0.0	0.0
40	2.9	2.6	3.3	80	0.0	0.0	0.0

IC208 (LM2940DCT-5.0) [V]

Pin No.	MODE		
	STOP	PLAY	REC
U	9.3	—	—
G	0.0	—	—
+5	5.0	—	—

IC311 (PST529C) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	5.0	5.0	5.0
2	0.0	0.0	0.0
3	5.0	5.0	5.0

IC204 (HD74HC4053EF) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	0.0	0.0	0.0
3	0.9	1.5	1.9
4	0.9	0.1	1.9
5	0.1	0.1	1.3
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	0.0	0.0	0.0
9	5.0	0.0	5.0
10	0.0	0.0	0.0
11	0.0	4.9	0.2
12	5.0	5.0	5.0
13	0.0	5.0	5.0
14	5.0	5.0	5.0
15	0.0	0.0	0.0
16	5.0	5.0	5.0

PCB-2

IC351 (PD4591A) [V]

Pin No.	MODE			Pin No.	MODE		
	STOP	PLAY	REC		STOP	PLAY	REC
1	−22.6	−22.0	−22.0	42	4.8	4.8	4.8
2	0.0	0.0	0.0	43	0.0	5.0	5.0
3	0.0	0.0	0.0	44	0.1	4.9	0.1
4	0.0	0.0	−22.0	45	5.0	0.0	0.1
5	−22.6	0.0	−22.0	46	0.08	0.0	0.1
6	0.0	−22.0	−22.0	47	0.08	0.0	0.1
7	−22.6	−22.0	−22.0	48	0.07	0.0	0.1
8	5.0	5.0	5.0	49	0.07	0.0	0.1
9	0.06	5.0	5.0	50	4.9	4.9	0.0
10	0.06	0.0	0 or 5	51	4.9	4.9	0.0
11	0.0	0.0	0.0	52	5.0	5.0	5.0
12	0.0	0.0	0.0	53	4.7	4.7	4.7
13	0.0	0.0	0.0	54	4.7	4.7	4.7
14	5.0	0.0	0.0	55	4.7	4.7	4.7
15	4.5	0.0	0.0	56	−23.6	−23.2	−23.2
16	0.8	0.0	0.0	57	−23.6	−23.3	−23.1
17	5.0	0.0	0.0	58	0.0	0.0	0.0
18	5.0	5.0	0.0	59	0.0	0.0	0.0
19	0.08	0.0	0.0	60	0.0	0.0	0.0
20	0.08	0.0	0.0	61	0.0	0.0	0.0
21	0.08	0.0	0.0	62	0.0	0.0	0.0
22	0.05	0.0	0.0	63	0.0	0.0	0.0
23	0.05	5.0	5.0	64	0.0	5.0	5.0
24	0.0	0.0	0.0	65	−24.6	−24.3	−16.0
25	5.0	5.0	5.0	66	−13.8	−13.6	−10.9
26	0.06	5.0	—	67	−21.8	−13.4	−13.3
27	0.06	0.0	0.0	68	−24.5	−24.4	−21.4
28	0.0	0.0	0.1	69	−24.6	−16.3	−16.2
29	0.06	0.0	0.1	70	−8.8	−13.3	−13.4
30	0.06	0.0	0.1	71	−25.0	−24.6	−24.7
31	0.0	0.0	0.1	72	−12.1	−11.7	(−12 to 14)
32	0.07	0.0	0.1				
33	0.07	0.0	0.1	73	−12.0	(−14.0 to 8.0)	0.0
34	0.07	0.0	0.1				
35	0.06	0.0	0.1	74	−9.6	−9.4	0.0
36	0.0	0.0	0.1	75	−9.6	−9.4	0.0
37	0.06	0.0	0.1	76	−12.1	−6.9	−9.3
38	0.06	0.0	0.1	77	−22.4	−22.1	−22.0
39	0.0	0.0	0.1	78	−22.4	−22.1	−22.0
40	0.05	4.9	4.9	79	−22.3	−22.0	−22.0
41	4.8	4.8	4.8	80	−22.4	−22.0	−22.0

IC352 (LC3517BML-15) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	2.8	2.7	2.7
2	0.7	1.4	1.1
3	3.8	3.3	3.7
4	2.7	2.0	2.5
5	4.0	3.4	3.7
6	3.6	3.0	2.6
7	3.2	2.5	2.6
8	1.5	0.9	1.1
9	2.7	3.3	3.1
10	3.0	3.1	3.3
11	3.2	3.1	3.0
12	0.0	0.0	0.0
13	3.3	3.4	3.2
14	1.8	1.8	2.0
15	3.4	3.3	3.4
16	1.2	1.5	1.4
17	2.9	2.7	2.8
18	4.5	4.5	4.5
19	0.9	0.8	1.1
20	4.9	4.9	4.9
21	4.9	4.9	4.9
22	2.7	2.5	2.5
23	2.8	2.8	2.9
24	4.6	4.6	4.5

IC353 (HD74HC573FP) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	2.7	3.4	3.1
3	3.0	3.2	3.4
4	3.2	3.2	3.0
5	3.2	3.3	3.2
6	1.9	1.8	2.1
7	3.5	3.1	3.3
8	1.2	1.4	1.4
9	2.8	2.7	2.7
10	0.0	0.0	0.0
11	0.1	0.1	0.1
12	2.8	2.7	3.0
13	0.8	1.6	1.0
14	3.9	3.5	3.7
15	0.3	1.9	2.9
16	4.1	3.0	3.4
17	3.6	3.2	2.2
18	3.2	2.3	2.2
19	1.5	0.9	1.4
20	5.0	5.0	5.0

IC354 (TC7S00F) [V]

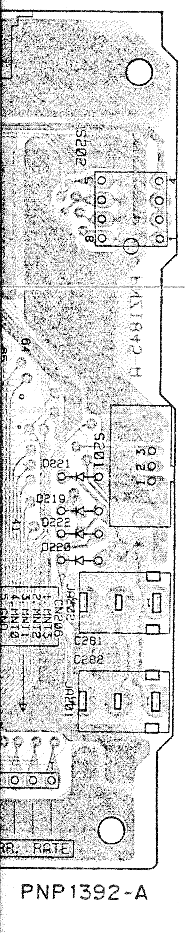
Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	4.9	4.9	4.9
3	0.0	0.0	0.0
4	4.5	4.5	4.5
5	4.5	4.5	4.5

IC355 (TC7S04F) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	4.9	5.0	5.0
3	0.0	0.0	0.0
4	0.0	0.0	0.0
5	5.0	5.0	5.0

IC356 (PD4584A) [V]

Pin No.	MODE			Pin No.	MODE		
	STOP	PLAY	REC		STOP	PLAY	REC
1	3.3	3.4	3.3	38	0.1	5.0	5.0
2	1.9	1.8	2.0	39	4.7	4.8	4.8
3	3.4	3.3	3.4	40	4.3	2.0	2.6
4	1.2	1.6	1.3	41	4.8	4.7	4.7
5	0.0	0.0	0.3	42	4.9	4.9	4.8
6	0.0	0.0	0.2	43	0.0	0.0	0.0
7	0.0	0.0	0.2	44	4.3	4.3	4.2
8	0.0	0.0	1.0	45	0.0	5.0	5.0
9	0.0	0.0	0.2	46	0.0	4.9	0.0
10	0.0	0.0	0.2	47	0.0	4.9	4.9
11	0.0	0.0	1.4	48	2.5	2.6	2.3
12	0.0	0.0	0.2	49	0.1	0.1	0.1
13	0.6	0.8	0.9	50	0.1	0.1	4.9
14	0.2	0.3	0.3	51	2.6	—	—
15	5.0	5.0	5.0	52	2.6	—	—
16	0.0	0.0	0.0	53	0.0	0.0	0.0
17	4.9	4.9	4.9	54	0.0	0.0	0.0
18	0.0	0.0	0.0	55	5.0	5.0	5.0
19	0.0	0.0	0.0	56	0.1	4.8	4.8
20	0.0	0.0	0.0	57	0.0	0.0	0.0
21	0.0	0.0	0.0	58	5.0	4.9	4.9
22	0.0	0.1	0.0	59	5.0	4.3	4.5
23	1.7	2.6	2.0	60	0.1	5.0	5.0
24	1.6	0.8	1.2	61	0.1	0.6	0.7
25	4.8	4.8	4.8	62	0.1	4.9	4.9
26	5.0	5.0	5.0	63	0.1	5.0	4.9
27	5.0	5.0	5.0	64	0.1	0.0	4.9
28	5.0	5.0	5.0	65	0.1	5.0	5.0
29	4.9	5.0	4.9	66	0.1	0.0	0.0
30	0.4	2.8	2.8	67	4.9	4.9	4.9
31	0.4	0.0	0.0	68	4.9	4.9	4.9
32	0.3	0.0	0.0	69	4.9	4.9	4.9
33	0.0	0.0	0.0	70	4.9	4.9	4.9
34	5.0	0.0	5.0	71	0.1	0.1	0.1
35	0.0	5.0	5.0	72	3.5	3.3	3.1
36	0.8	0.0	2.8	73	0.1	3.2	3.3
37	0.2	0.0	0.0	74	0.1	3.2	3.0



TO AUDIO DIGITAL BOARD ASSY CN302

PNP1392-A

IC357 (TC74HC367AF) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	4.4	4.3	4.3
2	0.0	0.0	0.0
3	0.0	0.0	0.0
4	4.5	4.4	4.4
5	4.5	2.3	2.3
6	5.4	5.0	5.0
7	4.7	2.5	2.5
8	0.0	0.0	0.0
9	4.8	4.8	4.7
10	4.8	4.8	4.8
11	0.0	0.0	0.0
12	0.0	0.0	0.0
13	4.8	4.7	4.7
14	4.5	4.4	4.5
15	4.5	4.4	4.5
16	5.0	5.0	5.0

IC360 (XL93LC46AF) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	5.0	5.0	5.0
3	0.0	0.0	0.0
4	4.9	4.8	4.8
5	4.3	2.2	2.2
6	4.8	4.7	4.7
7	0.0	0.0	0.0
8	0.0	0.0	0.0

IC5008 (BA4560F) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	−0.2	−0.5
2	0.0	0.0	0.0
3	0.0	0.0	0.0
4	−5.0	−5.0	−5.0
5	0.0	0.0	0.0
6	−0.0	−0.0	0.0
7	−0.0	0.1	−0.3
8	5.0	5.0	5.0

Q13 (DTC114TK) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	0.0	0.0
C	0.0	0.0	0.0
B	5.0	5.0	5.0

Q208 (DTC114TS) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	0.0	0.0
C	0.6	0.6	0.6
B	4.4	4.3	4.3

IC361 (PST572E) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	5.0	5.0	5.0
2	0.0	0.0	0.0
3	4.9	5.0	5.0

IC5024 (HD74HC4053FP) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.3	−0.5
2	0.0	0.0	0.0
3	0.0	0.0	0.0
4	0.0	0.0	0.0
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	−4.9	−4.9	−5.0
8	0.0	0.0	0.0
9	0.0	4.9	5.0
10	0.0	0.0	0.0
11	0.0	0.0	0.0
12	0.0	0.0	0.0
13	0.0	−0.7 to −0.2	−1.0 to −0.5
14	0.0	0.0	0.0
15	0.0	0.0	0.0
16	5.0	5.0	5.0

Q14 (DTA124EK) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	5.0	5.0	5.0
B	0.0	0.0	0.0

Q5026 (DTA124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	5.0	3.6	3.6
B	0.0	5.0	5.0

Q201 (DTA124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	0.0	0.0	3.4
B	5.0	5.0	2.8

IC358 (TC74HC367AF) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.6	0.6	0.6
2	4.9	4.9	4.8
3	4.9	4.9	—
4	4.9	4.9	4.8
5	4.8	4.8	4.7
6	4.3	1.8 to 2.3	2.2 to 2.7
7	4.7	2.5	2.5
8	0.0	0.0	0.0
9	4.4	2.2	2.2
10	4.4	2.2	2.3
11	4.8	4.7	4.7
12	0.0	4.6	4.6
13	5.0	4.9	4.9
14	4.9	4.8	4.8
15	5.0	4.8	4.8
16	5.0	5.0	5.0

IC362 (TC7S04F) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.2	0.0	0.1
2	5.0	0.0	5.0
3	0.0	0.0	0.0
4	0.0	5.0	0.0
5	5.0	5.0	5.0

IC363 (TC7S14F) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.2	0.0	0.1
2	0.0	5.0	0.0
3	0.0	0.0	0.0
4	5.0	0.0	5.0
5	5.0	5.0	5.0

Q202 (2SC2412K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	−3.8	0.0	3.9
C	−4.9	5.0	5.0
B	−4.7	4.6	4.6

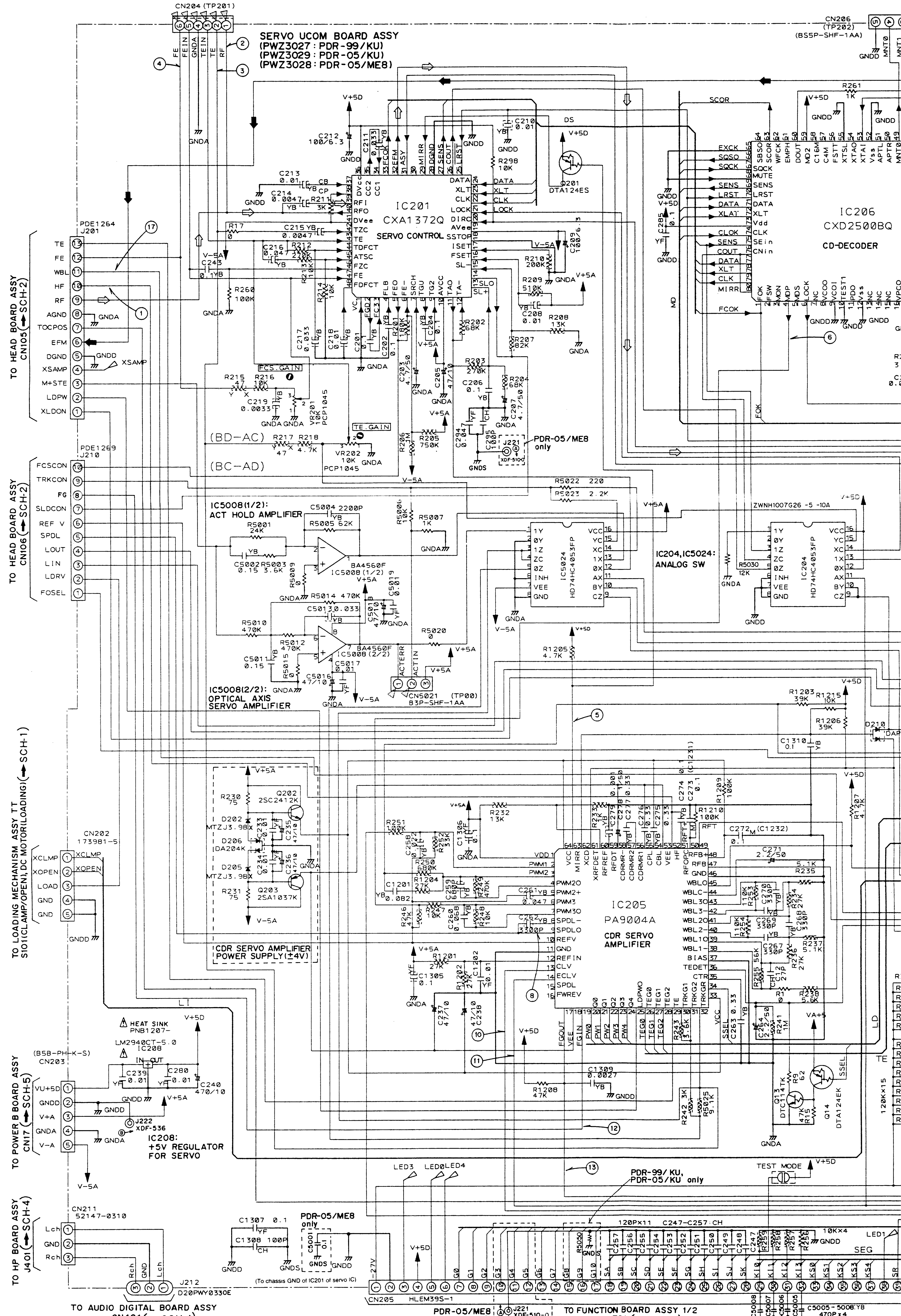
Q203 (2SA1037K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	3.9	−3.9	−3.9
C	5.0	−4.9	−4.9
B	4.6	−4.7	−4.7

IC359 (TC7S04F) [V]

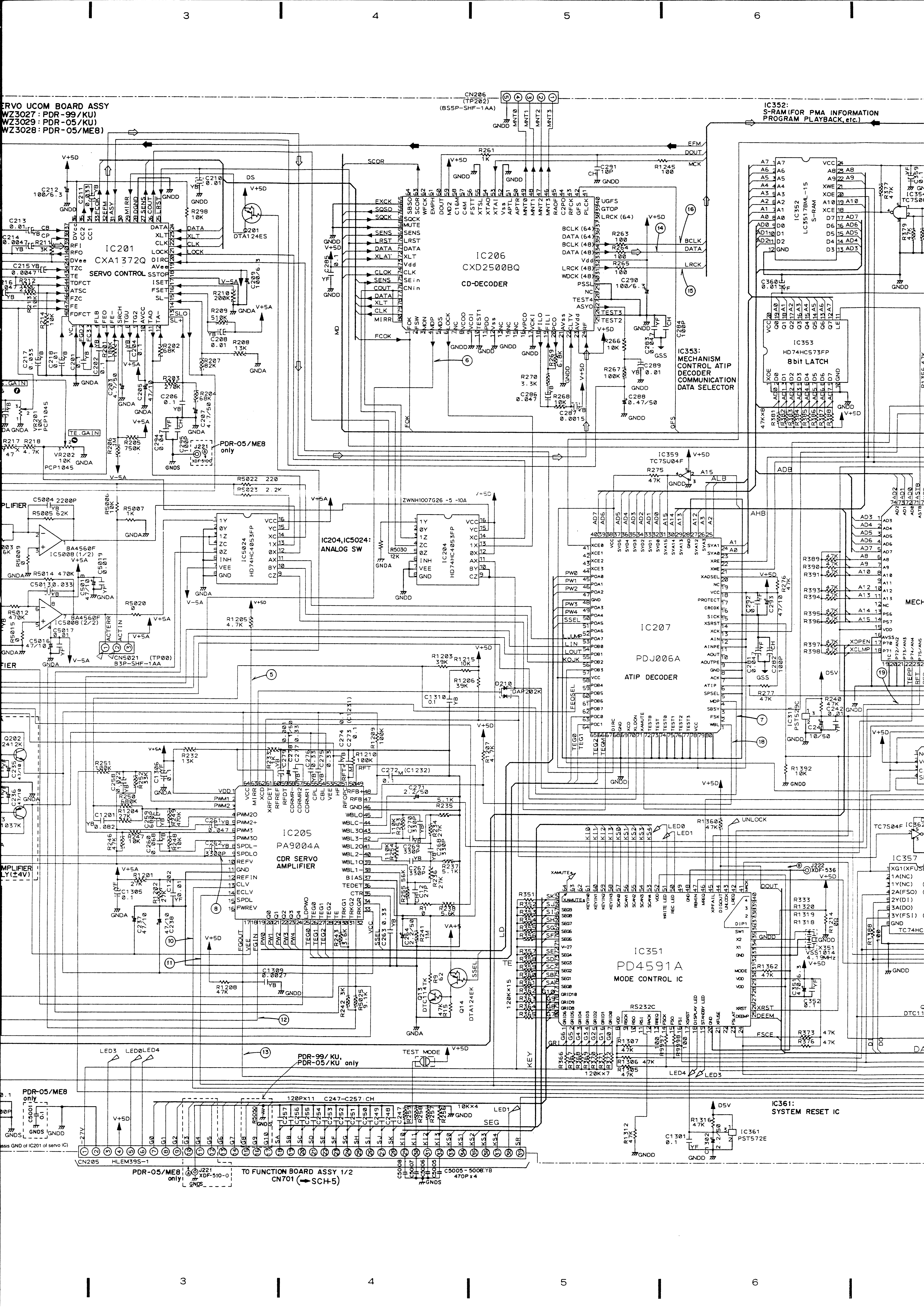
Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.1
2	0.2	0.3	0.3
3	0.0	0.0	0.0
4	4.7	4.7	4.7
5	5.0	5.0	5.0

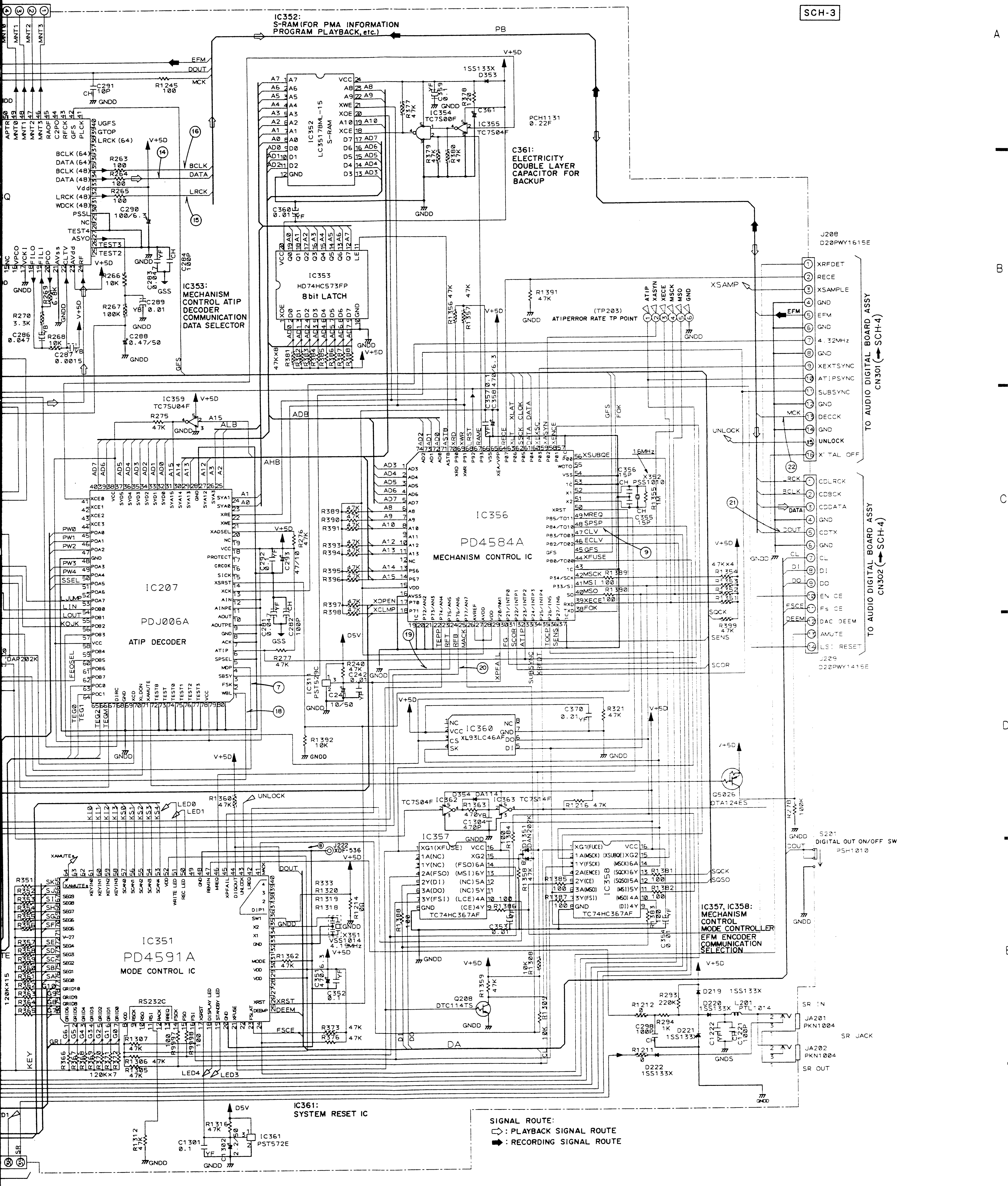
SY


1
2
3
4
B
C
D
E
F
SERVO UCOM BOARD ASSY
(PWZ3027 : PDR-99/KU)
(PWZ3029 : PDR-05/KU)
(PWZ3028 : PDR-05/ME8)
CN204 (TP201)
FE
FEIN
GNDA
TEIN
TE
RF
CN206 (TP202) (BS5P-SHF-1AA)
IC201
CXA1372Q
SERVO CONTROL
IC206
CXD2500BQ
CD-DECODER
Q201 DTA124ES
DS
SCOR
TO HEAD BOARD ASSY CN105 (→SCH-2)
PDE1264 J201
TE
FE
WBL
HF
RF
AGND
TOCPOS
EFM
DGND
XSAMP
M+STE
LDPW
XLDON
FCS.GAIN
TE.GAIN
VR201 PCP1045
VR202 10K PCP1045
(BD-AC)
(BC-AD)
TO HEAD BOARD ASSY CN106 (→SCH-2)
PDE1269 J210
FCSCON
TRKCON
FG
SLDCON
REF V
SPDL
LOUT
LIN
LDRV
FOSEL
IC5008(1/2): ACT HOLD AMPLIFIER
IC5008(2/2): OPTICAL AXIS SERVO AMPLIFIER
BA4560F
ACTERR
ACTIN
CN5021 (TP00) B3P-SHF-1AA
IC5024 HD74HC4053FP
IC204 HD74HC4053FP
IC204,IC5024: ANALOG SW
ZWNH1007G26 -5 -10A
PDR-05/ME8 only
J221 XDF-510
TO LOADING MECHANISM ASSY TT S101(CLAMP/OPEN), DC MOTOR(LOADING) (→SCH-1)
CN202 173981-5
XCLMP
XOPEN
LOAD
GND
GND
CDR SERVO AMPLIFIER POWER SUPPLY(±4V)
Q202 2SC2412K
Q203 2SA1037K
D202 MTZJ3.9B
D206 DA204K
D205 MTZJ3.9B
IC205
PA9004A
CDR SERVO AMPLIFIER
Q13 DTC114TK
Q14 DTA124EK
D210
TEST MODE
⚠ HEAT SINK PNB1207-
⚠ LM2940CT-5.0 IC208
IN OUT
IC208: +5V REGULATOR FOR SERVO
TO POWER B BOARD ASSY CN17 (→SCH-5)
(B5B-PH-K-S) CN203
VU+5D
GND
V+A
GNDA
V-A
J222 XDF-536
TO HP BOARD ASSY J401 (→SCH-4)
CN211 52147-0310
Lch
GND
Rch
J212 D20PWY0330E
TO AUDIO DIGITAL BOARD ASSY CN401 (→SCH-4)
C1307 0.1
C1308 100P
PDR-05/ME8 only
C5001 0.1
(To chassis GND of IC201 of servo IC)
LED3
LED0
LED4
PDR-99/KU, PDR-05/KU only
120P×11 C247-C257:CH
10K×4
LED1
SEG
CN205 HLEM39S-1
PDR-05/ME8 only
J221 XDF-510-0
TO FUNCTION BOARD ASSY 1/2 CN701 (→SCH-5)
C5005-5008:YB 470P×4
120K×15

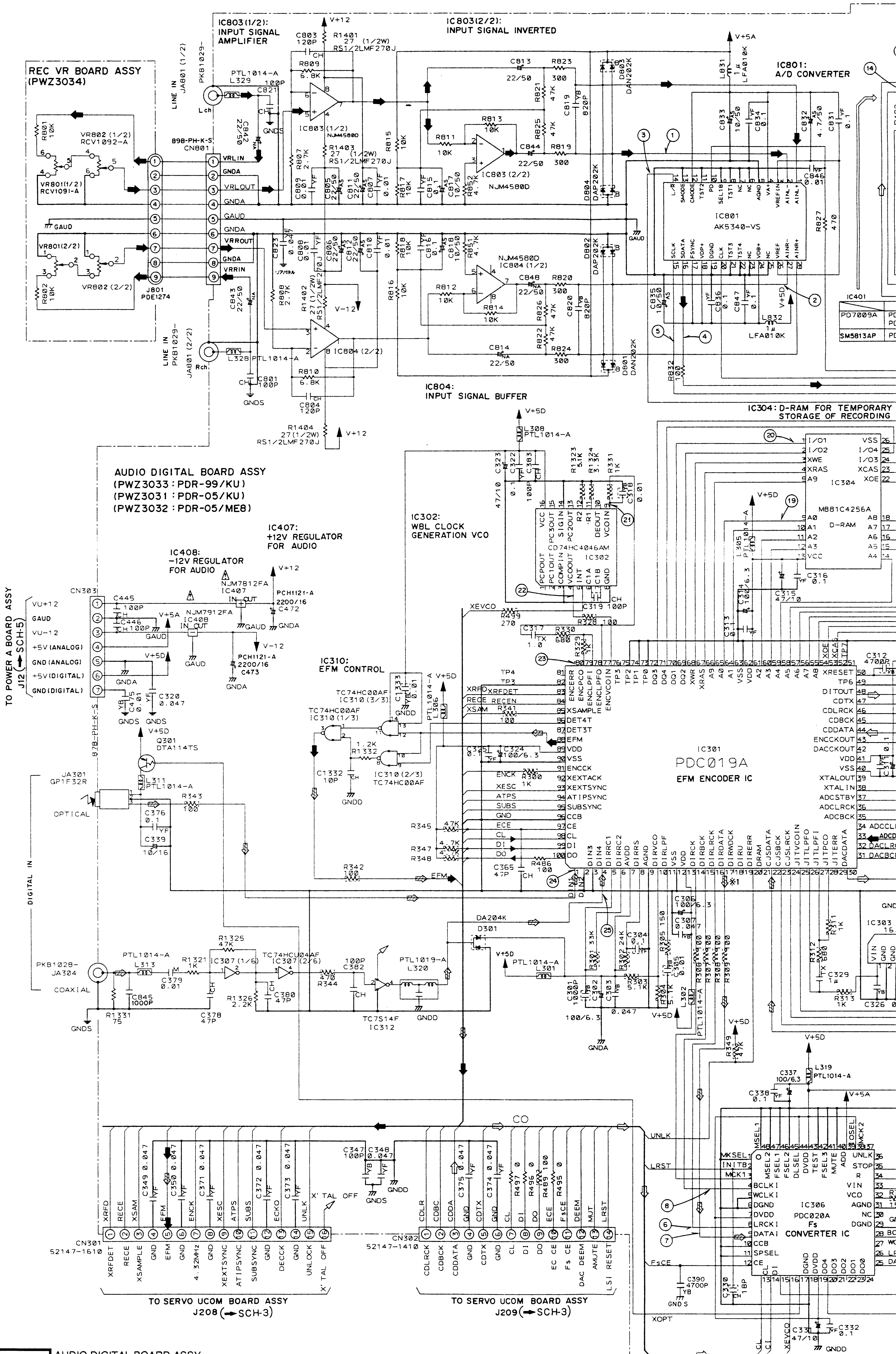
SCH-3

SERVO UCOM BOARD ASSY


3
4
5
6
SERVO UCOM BOARD ASSY
WZ3027 : PDR-99/KU)
WZ3029 : PDR-05/KU)
WZ3028 : PDR-05/ME8)
CN206 (TP202) (B5P-SHF-1AA)
MNT0
MNT1
MNT2
MNT3
GNDD
IC352:
S-RAM(FOR PMA INFORMATION PROGRAM PLAYBACK, etc.)
IC201
CXA1372Q
SERVO CONTROL
Q201
DTA124ES
IC206
CXD2500BQ
CD-DECODER
IC352
LC3517BML-15
S-RAM
IC353
HD74HC573FP
8bit LATCH
IC353:
MECHANISM CONTROL ATIP DECODER COMMUNICATION DATA SELECTOR
IC359
TC7SU04F
VR201 10K PCP1045
TE.GAIN
VR202 10K PCP1045
PDR-05/ME8 only
J221 XDF-510-0
IC5024
HD74HC4053FP
IC204
HD74HC4053FP
IC204,IC5024:
ANALOG SW
ZWNH1007G26 -5 -10A
BA4560F
IC5008 (1/2)
BA4560F
IC5008 (2/2)
CN5021 (TP00) B3P-SHF-1AA
ACTERR
ACTIN
IC207
PDJ006A
ATIP DECODER
D210
DAP202K
IC205
PA9004A
CDR SERVO AMPLIFIER
Q13
DTC114TK
Q14
DTA124EK
IC351
PD4591A
MODE CONTROL IC
RS232C
X351
VSS1014
4.19MHz
J222 XDF-536
UNLOCK
LED0
LED1
LED3
LED4
TEST MODE
PDR-99/KU,
PDR-05/KU only
120PX11 C247-C257:CH
10KX4
120KX15
120KX7
47KX8
SEG
KEY
IC361:
SYSTEM RESET IC
IC361
PST572E
IC357
TC74HC
TC7S04F
CN205 HLEM39S-1
PDR-05/ME8 only
TO FUNCTION BOARD ASSY 1/2
CN701 (→SCH-5)
C5005-5006:YB
470PX4
EFM
DOUT
MCK
SCOR
BCLK
DATA
LRCK
FCOK
MD
FOK
GFS
ADB
AHB
ALB
LD
TE
SSEL
MECH
V+5D
V+5A
V-5A
GNDD
GNDA
GNDS
GSS
D5V
VA+5
DA


SCH-3
IC352:
S-RAM(FOR PMA INFORMATION
PROGRAM PLAYBACK, etc.)
PB
IC352
LC3517BML-15
S-RAM
IC354
TC7S00F
IC355
TC7S04F
1SS133X
D353
PCH1131
0.22F
C361:
ELECTRICITY
DOUBLE LAYER
CAPACITOR FOR
BACKUP
IC353
HD74HC573FP
8bit LATCH
IC353:
MECHANISM
CONTROL ATIP
DECODER
COMMUNICATION
DATA SELECTOR
IC359
TC7SU04F
IC207
PDJ006A
ATIP DECODER
IC356
PD4584A
MECHANISM CONTROL IC
16MHz
X352
PSS1010
(TP203)
ATIPERROR RATE TP POINT
IC311
PST529C
IC360
XL93LC46AF
IC351
PD4591A
MODE CONTROL IC
X351
VSS1014
4.19MHz
RS232C
IC357
TC74HC367AF
IC358
TC74HC367AF
IC357, IC358:
MECHANISM
CONTROL
MODE CONTROLLER
EFM ENCODER
COMMUNICATION
SELECTION
Q208
DTC114TS
Q5026
DTA124ES
IC361:
SYSTEM RESET IC
IC361
PST572E
J208
D20PWY1615E
XRFDET
RECE
XSAMPLE
GND
EFM
GND
4.32MHz
GND
XEXTSYNC
ATIPSYNC
SUBSYNC
GND
DECCK
GND
UNLOCK
X'TAL OFF
TO AUDIO DIGITAL BOARD ASSY
CN301 (→ SCH-4)
CDLRCK
CDBCK
CDDATA
GND
CDTX
GND
CL
DI
DO
EN CE
Fs CE
DAC DEEM
AMUTE
LSI RESET
J209
D20PWY1415E
TO AUDIO DIGITAL BOARD ASSY
CN302 (→ SCH-4)
S201
DIGITAL OUT ON/OFF SW
PSH1010
SR IN
JA201
PKN1004
SR JACK
JA202
PKN1004
SR OUT
D219 1SS133X
D220 1SS133X
D221 1SS133X
D222 1SS133X
SIGNAL ROUTE:
⇨: PLAYBACK SIGNAL ROUTE
➡: RECORDING SIGNAL ROUTE

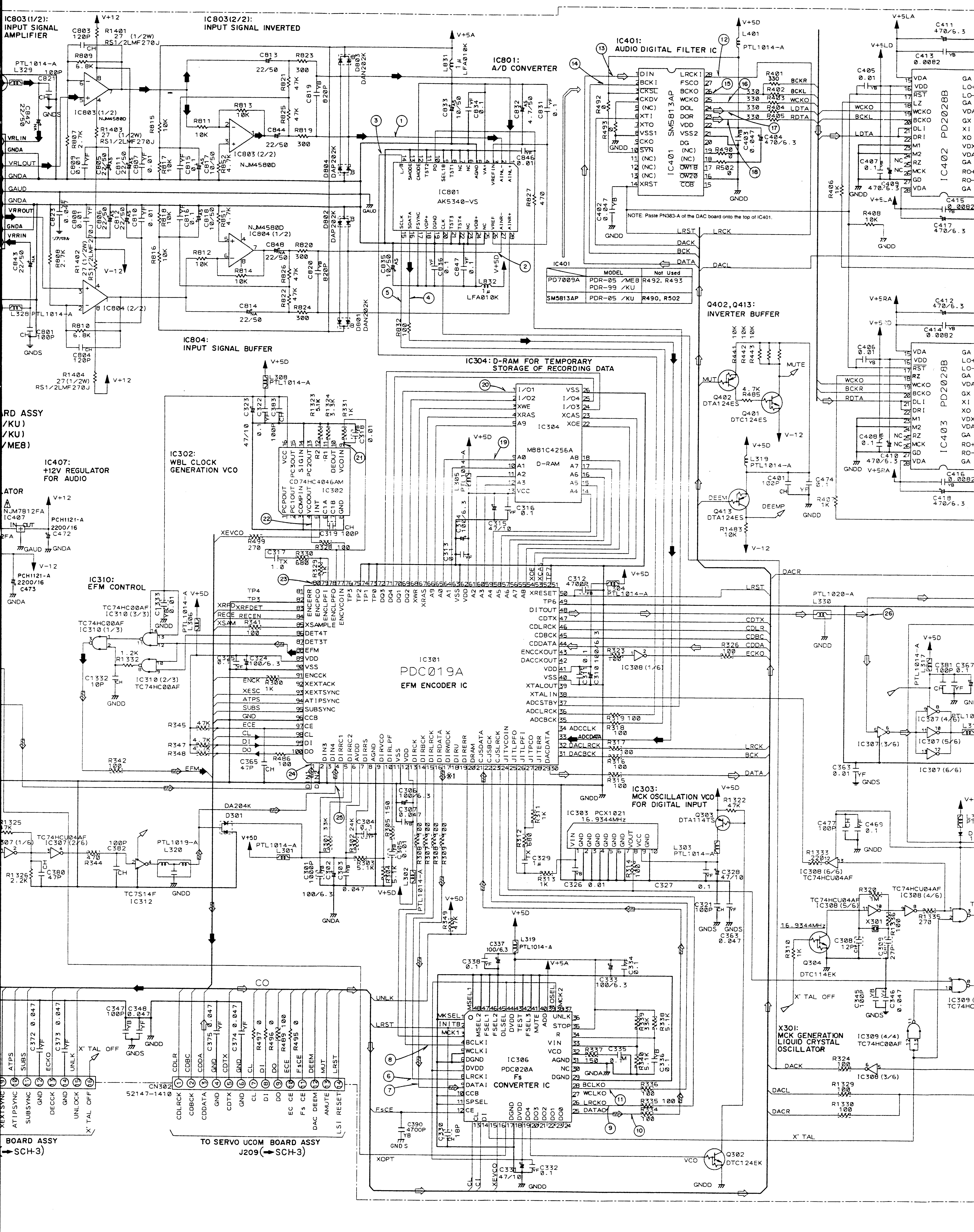
5.4 AUDIO DIGITAL BOARD, REC VR BOARD AND H.P BOARD ASSY


REC VR BOARD ASSY (PWZ3034)
VR802 (1/2) RCV1092-A
VR801(1/2) RCV1091-A
VR801(2/2)
VR802 (2/2)
J801 PDE1274
IC803(1/2): INPUT SIGNAL AMPLIFIER
IC803(2/2): INPUT SIGNAL INVERTED
IC804: INPUT SIGNAL BUFFER
IC801: A/D CONVERTER
AK5340-VS
LINE IN JA801 (1/2) PKB1029-
LINE IN JA801 (2/2) PKB1029-
Lch
Rch
898-PH-K-S CN801
VRLIN
GNDA
VRLOUT
GAUD
VRROUT
VRRIN
NJM4580D
DAP202K
DAN202K
LFA010K
IC401
PD7009A
SM5813AP
IC304: D-RAM FOR TEMPORARY STORAGE OF RECORDING
MB81C4256A
D-RAM
AUDIO DIGITAL BOARD ASSY
(PWZ3033 : PDR-99/KU)
(PWZ3031 : PDR-05/KU)
(PWZ3032 : PDR-05/ME8)
IC407: +12V REGULATOR FOR AUDIO
IC408: -12V REGULATOR FOR AUDIO
NJM7812FA
NJM7912FA
IC302: WBL CLOCK GENERATION VCO
CD74HC4046AM
IC310: EFM CONTROL
TC74HC00AF
IC301
PDC019A
EFM ENCODER IC
TO POWER A BOARD ASSY J12 (→SCH-5)
CN303
VU+12
GAUD
VU-12
+5V (ANALOG)
GND (ANALOG)
+5V (DIGITAL)
GND (DIGITAL)
Q301 DTA114TS
JA301 GP1F32R
OPTICAL
DIGITAL IN
PKB1028-JA304
COAXIAL
TC74HCU04AF
IC307
TC7S14F IC312
DA204K D301
IC303
IC306
PDC020A
Fs CONVERTER IC
CO
CN301 52147-1610
CN302 52147-1410
X' TAL OFF
XRFDET
RECE
XSAMPLE
GND
EFM
4.32MHz
XEXTSYNC
ATIPSYNC
SUBSYNC
DECCK
UNLOCK
CDLRCK
CDBCK
CDDATA
CDTX
DI
DO
EC CE
Fs CE
DAC DEEM
AMUTE
LSI RESET
TO SERVO UCOM BOARD ASSY J208 (→SCH-3)
TO SERVO UCOM BOARD ASSY J209 (→SCH-3)

SCH-4

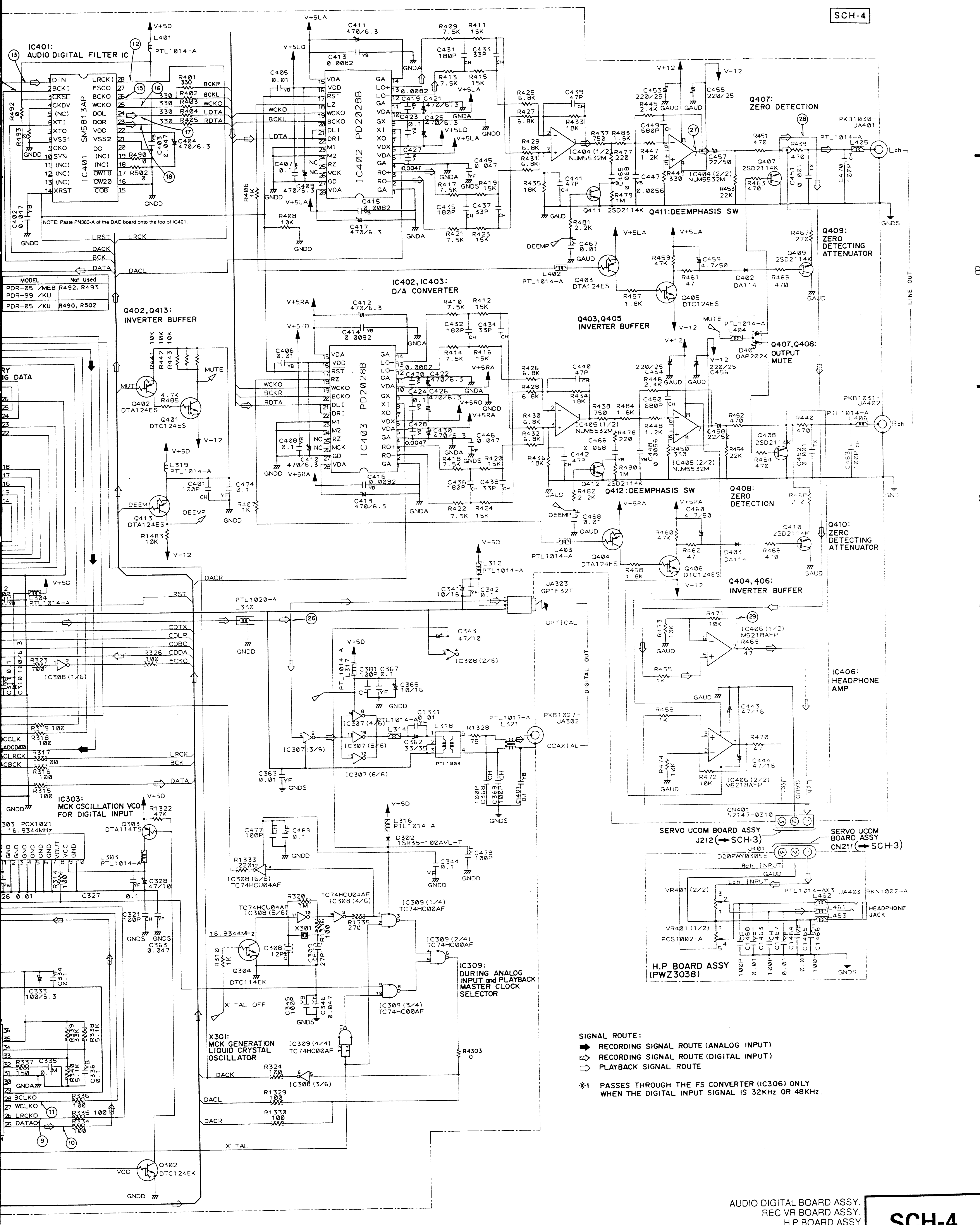
AUDIO DIGITAL BOARD ASSY,
REC VR BOARD ASSY,
H.P BOARD ASSY

RD AND H.P BOARD ASSY


IC803(1/2): INPUT SIGNAL AMPLIFIER
IC803(2/2): INPUT SIGNAL INVERTED
IC801: A/D CONVERTER
AK5340-VS
IC401: AUDIO DIGITAL FILTER IC
SM5813AP
IC402 PD2028B
IC403 PD2028B
IC804: INPUT SIGNAL BUFFER
NJM4580D
IC304: D-RAM FOR TEMPORARY STORAGE OF RECORDING DATA
MB81C4256A D-RAM
Q402,Q413: INVERTER BUFFER
DTA124ES
DTC124ES
MUTE
DEEMP
IC302: WBL CLOCK GENERATION VCO
CD74HC4046AM
IC407: +12V REGULATOR FOR AUDIO
NJM7812FA
IC310: EFM CONTROL
TC74HC00AF
IC301 PDC019A EFM ENCODER IC
IC303: MCK OSCILLATION VCO FOR DIGITAL INPUT
IC303 PCX1021 16.9344MHz
IC312 TC7S14F
IC307 TC74HCU04AF
IC306 PDC020A Fs CONVERTER IC
X301: MCK GENERATION LIQUID CRYSTAL OSCILLATOR
16.9344MHz
IC309 TC74HC00AF
IC308 TC74HCU04AF
Q302 DTC124EK
Q303 DTA114TS
Q304 DTC114EK
X' TAL OFF
CN302 52147-1410
TO SERVO UCOM BOARD ASSY J209(→SCH-3)
BOARD ASSY (→SCH-3)
XEXTSYNC
ATIPSYNC
SUBSYNC
GND
DECCK
GND
UNLOCK
X' TAL OFF
CDLRCK
CDBCK
CDDATA
GND
CDTX
GND
CL
DI
DO
EC CE
Fs CE
DAC DEEM
AMUTE
LSI RESET
CO
UNLK
LRST
DACK
DACL
DACR
X' TAL
XOPT
FsCE
VCO
RD ASSY (/KU) (/KU) (/ME8)

NOTE: Paste PN383-A of the DAC board onto the top of IC401.

IC401	MODEL	Not Used
PD7009A	PDR-05 /ME8 PDR-99 /KU	R492, R493
SM5813AP	PDR-05 /KU	R490, R502


SCH-4
IC401:
AUDIO DIGITAL FILTER IC
IC401 SM5813AP
NOTE: Paste PN383-A of the DAC board onto the top of IC401.
MODEL
Not Used
PDR-05 /ME8
PDR-99 /KU
R492, R493
PDR-05 /KU
R490, R502
Q402,Q413:
INVERTER BUFFER
IC402, IC403:
D/A CONVERTER
IC402 PD2028B
IC403 PD2028B
Q407:
ZERO DETECTION
Q411:DEEMPHASIS SW
Q409:
ZERO
DETECTING
ATTENUATOR
Q403,Q405
INVERTER BUFFER
Q407,Q408:
OUTPUT
MUTE
Q412:DEEMPHASIS SW
Q408:
ZERO
DETECTION
Q410:
ZERO
DETECTING
ATTENUATOR
Q404,406:
INVERTER BUFFER
IC406:
HEADPHONE
AMP
LINE OUT
Lch
Rch
PKB1030-JA401
PKB1031-JA402
JA303
GP1F32T
OPTICAL
DIGITAL OUT
COAXIAL
PKB1027-JA302
IC303:
MCK OSCILLATION VCO
FOR DIGITAL INPUT
IC309:
DURING ANALOG
INPUT and PLAYBACK
MASTER CLOCK
SELECTOR
X301:
MCK GENERATION
LIQUID CRYSTAL
OSCILLATOR
X' TAL OFF
SERVO UCOM BOARD ASSY
J212 (→SCH-3)
SERVO UCOM
BOARD ASSY
CN211 (→SCH-3)
CN401
52147-0310
J401
D20PWY0305E
H.P BOARD ASSY
(PWZ3038)
HEADPHONE
JACK
JA403 RKN1002-A
VR401 (2/2)
VR401 (1/2)
PCS1002-A
Rch INPUT
Lch INPUT

SIGNAL ROUTE:

- ➡ RECORDING SIGNAL ROUTE (ANALOG INPUT)
- ▨ RECORDING SIGNAL ROUTE (DIGITAL INPUT)
- ⇨ PLAYBACK SIGNAL ROUTE

※1 PASSES THROUGH THE FS CONVERTER (IC306) ONLY WHEN THE DIGITAL INPUT SIGNAL IS 32KHz OR 48KHz.

AUDIO DIGITAL BOARD ASSY,
REC VR BOARD ASSY,
H.P BOARD ASSY

SCH-4

C403 (PD2028BS) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	2.4	2.4	2.4
3	2.2	2.2	2.2
4	0.0	0.0	0.0
5	5.0	5.0	5.0
6	5.0	5.0	5.0
7	2.3	2.3	2.2
8	2.3	2.3	2.2
9	0.0	0.0	0.0
10	5.0	5.0	5.0
11	0.0	0.0	0.0
12	2.2	2.2	2.2
13	2.4	2.4	2.4
14	0.0	0.0	0.0
15	5.0	5.0	5.0
16	5.0	5.0	5.0
17	4.9	4.9	4.9
18	5.0	0.0	0.0
19	2.5	2.5	2.5
20	2.1	2.1	2.1
21	0.0	2.1	0.8
22	0.0	2.1	0.8
23	0.0	0.0	0.0
24	0.0	0.0	0.0
25	5.0	0.0	0.0
26	2.4	2.4	2.5
27	0.0	0.0	0.0
28	5.0	5.0	5.0

IC404 (NJM5532MD) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	1.2	1.2	1.2
3	1.2	1.2	1.2
4	– 12.1	– 12.1	– 12.1
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	11.9	11.9	11.9

IC405 (NJM5532MD) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	1.2	1.2	1.2
3	1.2	1.2	1.2
4	– 12.1	– 12.1	– 12.1
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	11.9	11.9	11.9

IC406 (M5218AFP) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	– 12.1	– 12.1	– 12.1
2	0.0	0.0	0.0
3	0.0	0.0	0.0
4	– 12.1	– 12.1	– 12.1
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	11.9	11.9	11.9

IC801 (AK5340-VS) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	2.5	2.5	2.5
2	2.5	2.5	2.5
3	5.0	5.0	2.4
4	5.0	5.0	0.0
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	0.0	0.0	0.0
9	0.0	0.0	0.0
10	5.0	5.0	0.0
11	0.0	0.0	0.0
12	5.0	5.0	5.0
13	0.0	0.0	0.0
14	2.5	2.5	2.5
15	2.0	2.0	2.2
16	0.0	0.0	2.5
17	5.0	5.0	5.0
18	5.0	5.0	5.0
19	0.0	0.0	0.0
20	2.1	2.1	2.1
21	0.0	0.0	0.0
22	0.0	0.0	0.0
23	0.0	0.0	0.0
24	5.0	5.0	5.0
25	0.0	0.0	0.0
26	5.0	5.0	2.4
27	2.5	2.5	2.5
28	2.5	2.5	2.5

IC803 (NJM4580D) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	0.0	0.0	0.0
3	0.0	0.0	0.0
4	– 12.0	– 12.0	– 12.0
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	11.8	11.8	11.8

IC804 (NJM4580D) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	0.0	0.0	0.0
3	0.0	0.0	0.0
4	– 12.0	– 12.0	– 12.0
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	11.8	11.8	11.8

Q301 (DTA114TS) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	0.5	0.4	0.4
B	5.0	5.0	5.0

Q302 (DTC124EK) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	0.0	0.0
C	5.0	5.0	5.0
B	0.0	0.0	0.0

Q303 (DTA114TS) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	0.9	0.8	0.8
B	5.0	5.0	5.0

Q304 (DTC114EK) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	0.0	0.0
C	2.0	—	—
B	0.2	– 0.1 to 0.0	0.0

Q401 (DTC124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	– 12.1	– 12.1	– 12.1
C	1.4	– 12.1	– 12.1
B	– 12.1	2.0	2.0

Q402 (DTA124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	– 12.1	5.0	5.0
B	5.0	3.6	3.6

Q403 (DTA124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	– 12.1	5.0	5.0
B	5.0	0.2	0.2

Q404 (DTA124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	– 12.1	5.0	5.0
B	5.0	0.2	0.2

Q405 (DTC124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	– 12.1	– 12.1	– 12.1
C	1.1	– 12.1	– 12.1
B	– 12.1	3.7	3.7

Q406 (DTC124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	– 12.1	– 12.1	– 12.1
C	1.1	– 12.1	– 12.1
B	– 12.1	3.7	3.7

Q408 (2SD2114K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	0.0	0.0
C	0.0	0.0	0.0
B	0.6	– 0.7	– 0.1

Q410 (2SD2114K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	0.0	0.0
C	0.0	0.0	0.0
B	0.6	– 0.8	– 0.2

Q412 (2SD2114K) [V]

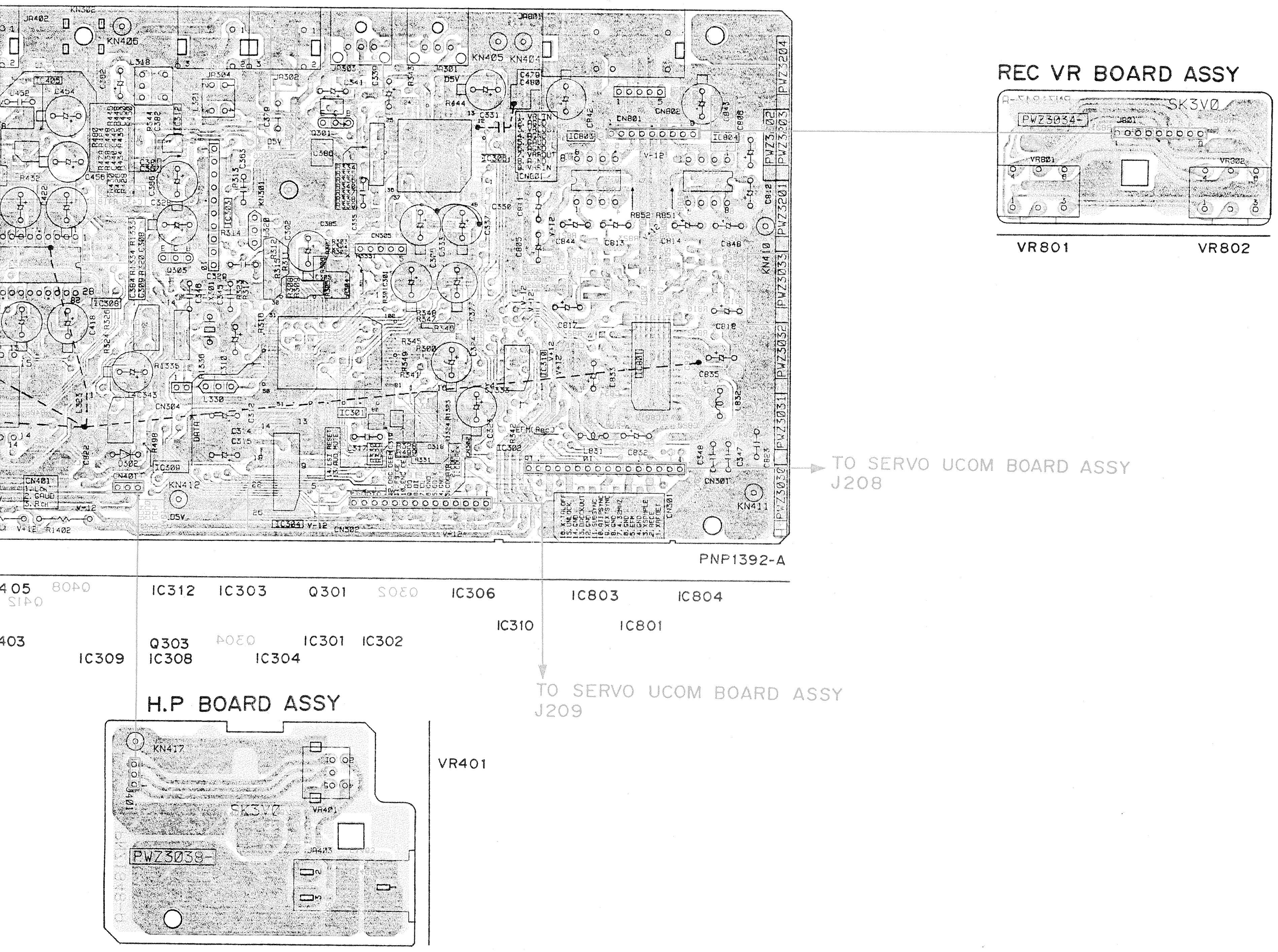
Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	0.0	0.0
C	0.0	0.0	0.0
B	– 12.1	– 12.1	– 12.1

Q413 (DTA124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	– 12.1	– 12.1	– 12.1
B	5.0	5.0	5.0

- The parts mounted on this PCB include all necessary parts for several destinations. For further information for respective destinations, be sure to check with the schematic diagram.

PCB-3



C309 (TC74HC00AF) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	2.0	2.2	2.2
2	4.8	5.0	5.0
3	1.5	2.0	2.0
4	0.9 to 1.8	2.0	2.1
5	4.2	4.3	4.3
6	2.2	2.3	2.3
7	0.0	0.0	0.0
8	4.2	4.3	4.3
9	0.0	0.0	0.0
10	0.0	0.0	0.0
11	0.0	0.0	0.0
12	4.8	5.0	4.9
13	4.8	5.0	4.9
14	4.2	4.3	4.3

C310 (TC74HC00AF) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	5.0	5.0	3.0
2	5.0	5.0	4.6
3	0.0	0.0	2.0
4	0.0	0.0	0.0
5	0.0	0.0	0.0
6	5.0	5.0	5.0
7	0.0	0.0	0.0
8	5.0	5.0	4.6
9	0.0	0.0	0.6
10	0.0	0.0	1.9
11	5.0	5.0	3.0
12	0.0	0.0	2.0
13	5.0	5.0	5.0
14	5.0	5.0	5.0

C312 (TC7S14F) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	3.1	3.1	3.1
3	0.0	0.0	0.0
4	0.0	0.0	0.0
5	5.0	5.0	5.0

IC401 (PD7009A) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	1.6	2.4
2	2.1	2.1	2.2
3	4.9	5.0	5.0
4	4.8	4.9	4.9
5	4.8	4.9	4.9
6	2.0	2.1	2.2
7	2.8	2.8	2.8
8	0.0	0.0	0.0
9	2.1	2.1	2.2
10	4.8	4.9	4.9
11	4.8	4.9	4.9
12	4.8	4.9	4.9
13	4.8	4.9	4.9
14	4.9	4.9	4.9
15	4.9	5.0	5.0
16	0.0	0.0	0.0
17	4.8	4.9	4.9
18	0.0	0.0	0.0
19	0.0	0.0	0.0
20	4.8	4.9	4.9
21	0.0	0.0	0.0
22	4.9	5.0	5.0
23	0.0	2.1	2.1
24	0.0	2.1	2.1
25	2.5	2.5	2.5
26	2.0	2.0	2.0
27	4.8	4.9	4.9
28	2.5	2.5	2.5

IC402 (PD2028BS) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	2.4	2.4	2.4
3	2.2	2.2	2.2
4	0.0	0.0	0.0
5	5.0	5.0	5.0
6	5.0	5.0	5.0
7	2.3	2.3	2.3
8	2.3	2.3	2.3
9	0.0	0.0	0.0
10	5.0	5.0	5.0
11	0.0	0.0	0.0
12	2.2	2.2	2.2
13	2.4	2.4	2.4
14	0.0	0.0	0.0
15	5.0	5.0	5.0
16	5.0	5.0	5.0
17	4.9	4.9	4.9
18	5.0	0.0	0.0
19	2.5	2.5	2.5
20	2.1	2.1	2.1
21	0.0	2.1	0.8
22	0.0	2.1	0.8
23	0.0	0.0	0.0
24	0.0	0.0	0.0
25	5.0	0.0	0.0
26	2.4	2.4	2.5
27	0.0	0.0	0.0
28	5.0	5.0	5.0

IC403 (PD2028BS) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	2.4	2.4	2.4
3	2.2	2.2	2.2
4	0.0	0.0	0.0
5	5.0	5.0	5.0
6	5.0	5.0	5.0
7	2.3	2.3	2.2
8	2.3	2.3	2.2
9	0.0	0.0	0.0
10	5.0	5.0	5.0
11	0.0	0.0	0.0
12	2.2	2.2	2.2
13	2.4	2.4	2.4
14	0.0	0.0	0.0
15	5.0	5.0	5.0
16	5.0	5.0	5.0
17	4.9	4.9	4.9
18	5.0	0.0	0.0
19	2.5	2.5	2.5
20	2.1	2.1	2.1
21	0.0	2.1	0.8
22	0.0	2.1	0.8
23	0.0	0.0	0.0
24	0.0	0.0	0.0
25	5.0	0.0	0.0
26	2.4	2.4	2.5
27	0.0	0.0	0.0
28	5.0	5.0	5.0

IC404 (NJM5532MD) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	1.2	1.2	1.2
3	1.2	1.2	1.2
4	− 12.1	− 12.1	− 12.1
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	11.9	11.9	11.9

IC405 (NJM5532MD) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	1.2	1.2	1.2
3	1.2	1.2	1.2
4	− 12.1	− 12.1	− 12.1
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	11.9	11.9	11.9

IC406 (M5218AFP) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	− 12.1	− 12.1	− 12.1
2	0.0	0.0	0.0
3	0.0	0.0	0.0
4	− 12.1	− 12.1	− 12.1
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	11.9	11.9	11.9

IC801 (AK5340-VS) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	2.5	2.5	2.5
2	2.5	2.5	2.5
3	5.0	5.0	2.4
4	5.0	5.0	0.0
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	0.0	0.0	0.0
9	0.0	0.0	0.0
10	5.0	5.0	0.0
11	0.0	0.0	0.0
12	5.0	5.0	5.0
13	0.0	0.0	0.0
14	2.5	2.5	2.5
15	2.0	2.0	2.2
16	0.0	0.0	2.5
17	5.0	5.0	5.0
18	5.0	5.0	5.0
19	0.0	0.0	0.0
20	2.1	2.1	2.1
21	0.0	0.0	0.0
22	0.0	0.0	0.0
23	0.0	0.0	0.0
24	5.0	5.0	5.0
25	0.0	0.0	0.0
26	5.0	5.0	2.4
27	2.5	2.5	2.5
28	2.5	2.5	2.5

IC803 (NJM4580D) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	0.0	0.0	0.0
3	0.0	0.0	0.0
4	− 12.0	− 12.0	− 12.0
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	11.8	11.8	11.8

IC804 (NJM4580D) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	0.0	0.0	0.0
3	0.0	0.0	0.0
4	− 12.0	− 12.0	− 12.0
5	0.0	0.0	0.0
6	0.0	0.0	0.0
7	0.0	0.0	0.0
8	11.8	11.8	11.8

Q301 (DTA114TS) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	0.5	0.4	0.4
B	5.0	5.0	5.0

Q302 (DTC124EK) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	0.0	0.0
C	5.0	5.0	5.0
B	0.0	0.0	0.0

Q303 (DTA114TS) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	0.9	0.8	0.8
B	5.0	5.0	5.0

Q304 (DTC114EK) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	0.0	0.0
C	2.0	—	—
B	0.2	− 0.1 to 0.0	0.0

Q401 (DTC124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	− 12.1	− 12.1	− 12.1
C	1.4	− 12.1	− 12.1
B	− 12.1	2.0	2.0

Q402 (DTA124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	− 12.1	5.0	5.0
B	5.0	3.6	3.6

Q403 (DTA124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	− 12.1	5.0	5.0
B	5.0	0.2	0.2

Q404 (DTA124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	5.0	5.0	5.0
C	− 12.1	5.0	5.0
B	5.0	0.2	0.2

Q405 (DTC124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	− 12.1	− 12.1	− 12.1
C	1.1	− 12.1	− 12.1
B	− 12.1	3.7	3.7

Q406 (DTC124ES) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	− 12.1	− 12.1	− 12.1
C	1.1	− 12.1	− 12.1
B	− 12.1	3.7	3.7

Q408 (2SD2114K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	0.0	0.0
C	0.0	0.0	0.0
B	0.6	− 0.7	− 0.1

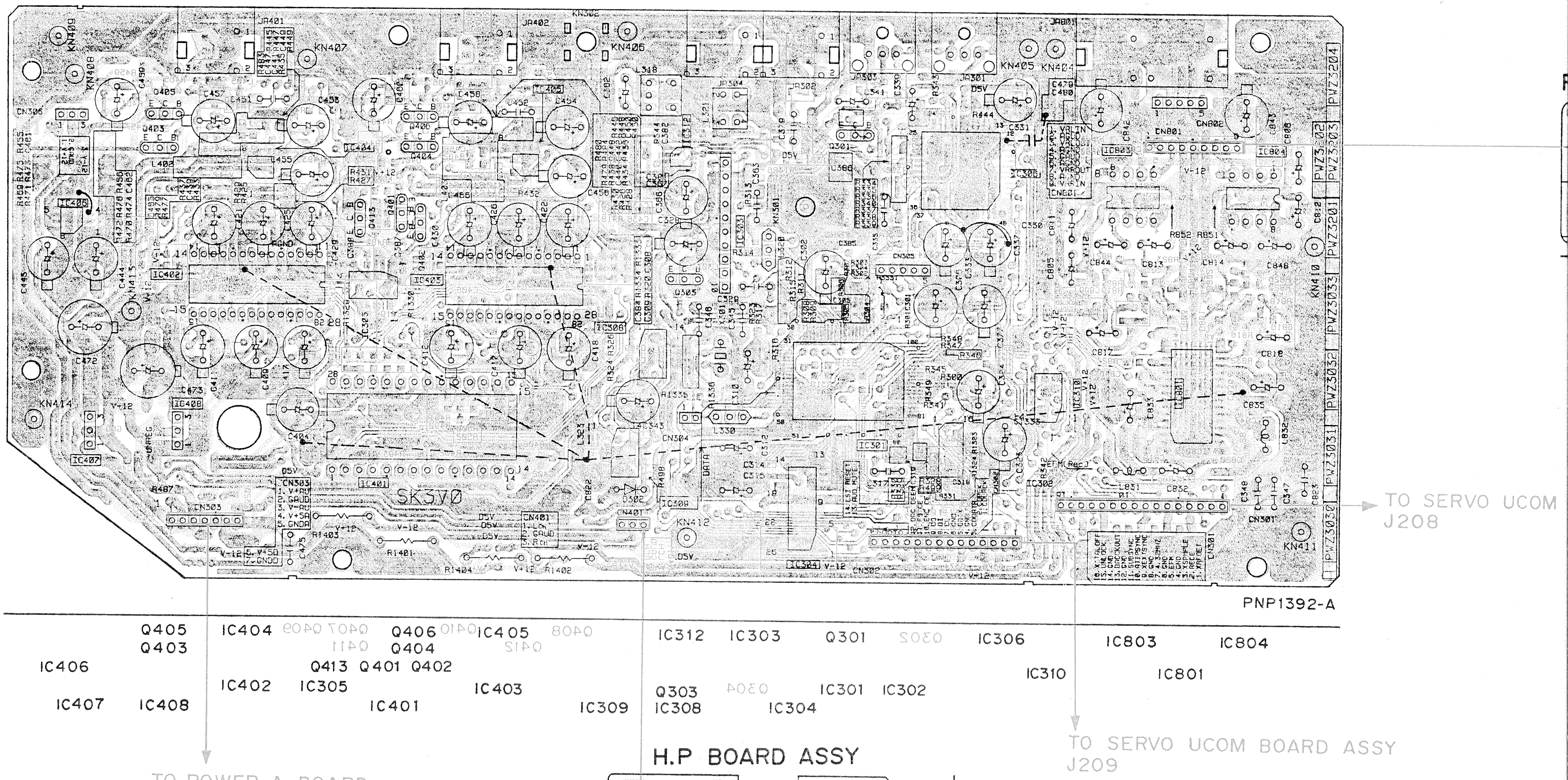
Q410 (2SD2114K) [V]

Pin No.	MODE		
	STOP	PLAY	REC
E	0.0	0.0	0.0
C	0.0	0.0	0.0
B	0.6	− 0.8	− 0.2

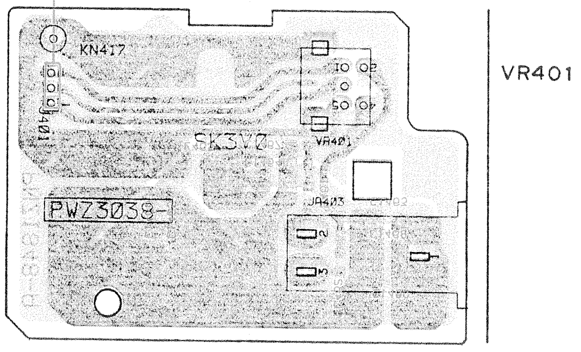
This diagram is viewed from the pink colored foil side.
This PCB is double sided.

- The parts mounted on this PCB include all necessary parts for several destinations. For further information for respective destinations, be sure to check with the schematic diagram.

AUDIO DIGITAL BOARD ASSY



H.P BOARD ASSY



Voltages (V) of AUDIO DIGITAL BOARD Assy

IC301 (PDC019A) [V]

Pin No.	MODE			Pin No.	MODE		
	STOP	PLAY	REC		STOP	PLAY	REC
1	0.0	0.0	0.0	50	4.9	4.9	4.9
2	0.0	0.0	0.0	51	0.0	0.0	0.0
3	0.0	0.0	0.0	52	5.0	5.0	3.9
4	0.0	0.0	0.0	53	5.0	5.0	4.1
5	2.4	2.4	2.4	54	0.0	0.0	2.3
6	2.4	2.4	2.4	55	0.0	0.0	2.3
7	5.0	5.0	5.0	56	0.0	0.0	2.4
8	1.8	1.8	1.8	57	0.0	0.0	2.5
9	0.0	0.0	0.0	58	0.0	0.0	2.5
10	2.5	2.5	2.5	59	0.0	0.0	2.5
11	2.5	2.5	2.5	60	0.0	0.0	2.4
12	0.0	0.0	0.0	61	5.0	5.0	5.0
13	5.0	5.0	5.0	62	0.0	0.0	0.0
14	2.0	2.3	2.4	63	0.0	0.0	1.4
15	0.0	0.0	0.0	64	0.0	0.0	1.3
16	0.0	0.0	0.0	65	0.0	0.0	2.4
17	0.0	0.0	0.0	66	5.0	5.0	2.0
18	0.0	5.0	5.0	67	5.0	5.0	4.1
19	0.0	5.0	5.0	68	0.0	0.0	0.9
20	5.0	5.0	5.0	69	0.0	0.0	0.8
21	0.0	0.0	0.0	70	0.0	0.0	0.0
22	0.0	0.0	0.0	71	0.0	0.0	0.7
23	0.0	0.0	0.0	72	0.0	0.0	0.0
24	0.0	0.0	0.0	73	0.0	0.0	0.0
25	0.0	0.0	0.1	74	0.0	0.0	0.0
26	2.4	2.4	5.0	75	5.0	5.0	5.0
27	2.4	2.4	0.0 to 3.4	76	2.6	0.0	2.5
				77	2.7	5.0	2.7
28	2.4	2.4	0.0 to 2.4	78	2.4	0.0	2.4
				79	2.4	0.0	2.4
29	5.0	5.0	5.0	80	0.0	5.0	0.0
30	0.0	1.6	0.0	81	0.0	0.0	0.0
31	2.0	2.0	2.2	82	0.0	0.0	0.0
32	2.5	0.0	2.5	83	5.0	0.0	5.0
33	0.0	0.0	0.6	84	0.0	0.0	4.9
34	0.0	0.6	0.6	85	0.0	0.0	3.1
35	2.0	2.0	2.0	86	0.0	0.0	0.6
36	0.0	2.5	2.5	87	0.0	0.0	0.7
37	0.0	5.0	0.0	88	0.0	0.0	1.9
38	2.2	2.2	2.2	89	5.0	5.0	5.0
39	2.7	2.7	2.6	90	0.0	0.0	0.0
40	0.0	0.0	0.0	91	1.4	5.0	1.3
41	5.0	5.0	5.0	92	5.0	5.0	5.0
42	2.0	2.0	2.2	93	5.0	4.9	4.9
43	2.0	2.2	2.2	94	0.2	0.0	0.3
44	0.0	2.4	0.0	95	0.0	0.0	0.0
45	2.0	2.0	2.0	96	0.0	0.0	0.0
46	2.5	2.5	2.5	97	4.8	4.8	4.8
47	2.4	2.4	2.4	98	4.9	4.8	4.8
48	2.0	2.0	2.1	99	0.6	2.3	2.3
49	0.0	0.0	0.0	100	5.0	5.0	5.0

IC302 (CD74HC4046AM) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	5.0	5.0	5.0
2	0.0	0.0	0.0
3	0.0	0.0	0.0
4	2.5	0.0	2.5
5	0.0	5.0	0.0
6	0.7	0.0	0.6
7	0.0	0.0	0.0
8	0.0	0.0	0.0
9	2.7	5.0	2.7
10	2.7	0.0	2.7
11	2.7	0.0	2.7
12	4.4	0.0	4.4
13	0.0	0.0	0.0
14	0.0	0.0	0.0
15	0.0	0.0	5.0
16	5.0	5.0	5.0

IC304 (MB81C4256A) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	1.4
2	0.0	0.0	1.4
3	5.0	5.0	4.1
4	5.0	5.0	2.0
5	0.0	0.0	2.5
6			
7			
8			
9	0.0	0.0	1.3
10	0.0	0.0	1.4
11	0.0	0.0	2.5
12	0.0	0.0	2.5
13	5.0	5.0	5.0
14	0.0	0.0	2.5
15	0.0	0.0	2.5
16	0.0	0.0	2.5
17	0.0	0.0	2.5
18	0.0	0.0	2.5
19			
20			
21			
22	5.0	5.0	4.1
23	5.0	5.0	3.9
24	0.0	0.0	0.9
25	0.0	0.0	0.8
26	0.0	0.0	0.0

IC306 (PDC020A) [V]

Pin No.	MODE			Pin No.	MODE		
	STOP	PLAY	REC		STOP	PLAY	REC
1	0.0	0.0	0.0	25	0.0	0.0	0.0
2	4.9	4.9	4.9	26	0.0	0.0	0.0
3	2.2	2.2	2.3	27	0.0	0.0	0.0
4	0.0	0.0	0.0	28	0.0	0.0	0.0
5	0.0	0.0	0.0	29	0.0	0.0	0.0
6	0.0	0.0	0.0	30	0.0	0.0	0.0
7	5.0	5.0	5.0	31	0.0	0.0	0.0
8	0.0	0.0	0.0	32	5.0	5.0	5.0
9	0.0	0.0	0.0	33	2.5	2.5	2.5
10	0.0	0.0	0.0	34	1.8	1.8	1.8
11	0.0	0.0	0.0	35	5.0	5.0	5.0
12	5.0	5.0	5.0	36	5.0	5.0	5.0
13	4.9	4.8	4.8	37	5.0	5.0	5.0
14	0.6	1.8 to 2.3	2.4	38	5.0	5.0	5.0
				39	5.0	5.0	5.0
15	5.0	5.0	5.0	40	0.0	0.0	0.0
16	0.0	5.0	0.0	41	0.0	0.0	0.0
17	5.0	5.0	5.0	42	0.0	0.0	0.0
18	0.0	0.0	0.0	43	5.0	5.0	5.0
19	5.0	5.0	5.0	44	5.0	5.0	5.0
20	0.0	0.0	0.0	45	0.0	0.0	0.0
21	0.0	0.0	0.0	46	0.0	0.0	0.0
22	0.0	0.0	0.0	47	0.0	0.0	0.0
23	0.0	0.0	0.0	48	0.0	0.0	0.0
24	0.0	0.0	0.0				

IC307 (TC74HCU04AF) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	2.5	2.5	2.5
2	2.5	2.5	2.5
3	2.5	2.6	2.6
4	3.1	3.1	3.1
5	2.2	2.0	2.0
6	2.6	2.6	2.6
7	0.0	0.0	0.0
8	2.4	2.4	2.4
9	2.6	2.6	2.6
10	2.4	2.4	2.4
11	2.6	2.6	2.6
12	2.4	2.4	2.4
13	2.6	2.6	2.6
14	5.0	5.0	5.0

IC308 (TC74HCU04AF) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	2.2	2.2	2.3
2	2.1	2.1	2.1
3	0.0	0.0	0.0
4	4.3	4.3	4.3
5	2.0	2.2	2.3
6	2.0	2.1	2.1
7	0.0	0.0	0.0
8	2.2	2.2	2.3
9	2.1	2.2	—
10	2.0	—	—
11	1.9	—	—
12	1.4	—	—
13	2.0	2.2	2.2
14	4.2	4.3	4.3

IC309 (TC74HC00AF) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	2.0	2.2	2.2
2	4.8	5.0	5.0
3	1.5	2.0	2.0
4	0.9 to 1.8	2.0	2.1
5	4.2	4.3	4.3
6	2.2	2.3	2.3
7	0.0	0.0	0.0
8	4.2	4.3	4.3
9	0.0	0.0	0.0
10	0.0	0.0	0.0
11	0.0	0.0	0.0
12	4.8	5.0	4.9
13	4.8	5.0	4.9
14	4.2	4.3	4.3

IC310 (TC74HC00AF) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	5.0	5.0	3.0
2	5.0	5.0	4.6
3	0.0	0.0	2.0
4	0.0	0.0	0.0
5	0.0	0.0	0.0
6	5.0	5.0	5.0
7	0.0	0.0	0.0
8	5.0	5.0	4.6
9	0.0	0.0	0.6
10	0.0	0.0	1.9
11	5.0	5.0	3.0
12	0.0	0.0	2.0
13	5.0	5.0	5.0
14	5.0	5.0	5.0

IC312 (TC7S14F) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	3.1	3.1	3.1
3	0.0	0.0	0.0
4	0.0	0.0	0.0
5	5.0	5.0	5.0

IC401 (PD7009A) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	1.6	2.4
2	2.1	2.1	2.2
3	4.9	5.0	5.0
4	4.8	4.9	4.9
5	4.8	4.9	4.9
6	2.0	2.1	2.2
7	2.8	2.8	2.8
8	0.0	0.0	0.0
9	2.1	2.1	2.2
10	4.8	4.9	4.9
11	4.8	4.9	4.9
12	4.8	4.9	4.9
13	4.8	4.9	4.9
14	4.9	4.9	4.9
15	4.9	5.0	5.0
16	0.0	0.0	0.0
17	4.8	4.9	4.9
18	0.0	0.0	0.0
19	0.0	0.0	0.0
20	4.8	4.9	4.9
21	0.0	0.0	0.0
22	4.9	5.0	5.0
23	0.0	2.1	2.1
24	0.0	2.1	2.1
25	2.5	2.5	2.5
26	2.0	2.0	2.0
27	4.8	4.9	4.9
28	2.5	2.5	2.5

IC402 (PD2028BS) [V]

Pin No.	MODE		
	STOP	PLAY	REC
1	0.0	0.0	0.0
2	2.4	2.4	2.4
3	2.2	2.2	2.2
4	0.0	0.0	0.0
5	5.0	5.0	5.0
6	5.0	5.0	5.0
7	2.3	2.3	2.3
8	2.3	2.3	2.3
9	0.0	0.0	0.0
10	5.0	5.0	5.0
11	0.0	0.0	0.0
12	2.2	2.2	2.2
13	2.4	2.4	2.4
14	0.0	0.0	0.0
15	5.0	5.0	5.0
16	5.0	5.0	5.0
17	4.9	4.9	4.9
18	5.0	0.0	0.0
19	2.5	2.5	2.5
20	2.1	2.1	2.1
21	0.0	2.1	0.8
22	0.0	2.1	0.8
23	0.0	0.0	0.0
24	0.0	0.0	0.0
25	5.0	0.0	0.0
26	2.4	2.4	2.5
27	0.0	0.0	0.0
28	5.0	5.0	5.0

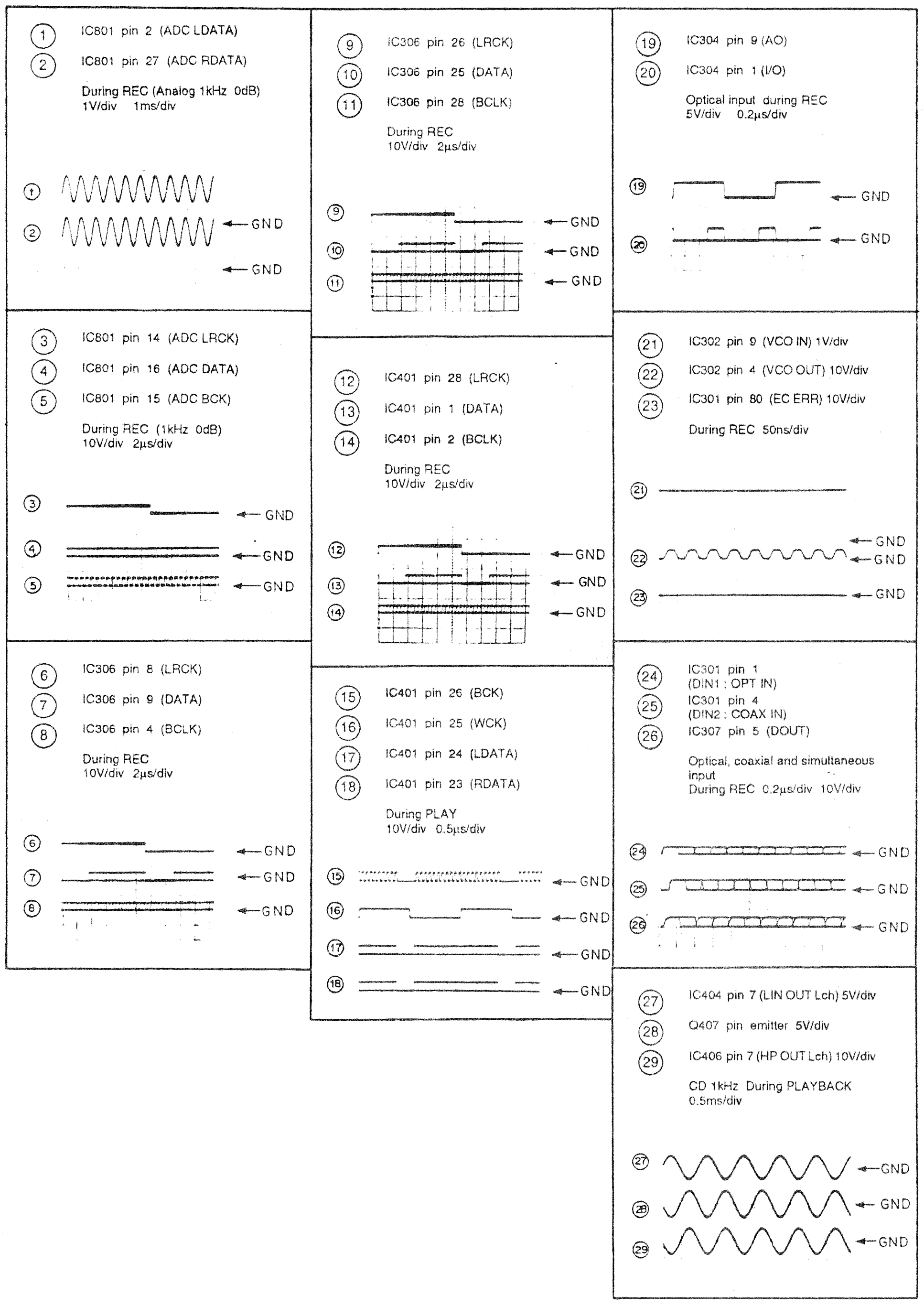
IC403 (PD

Pin No.	
	STOP
1	0
2	2
3	2
4	0
5	5
6	5
7	2
8	2
9	0
10	5
11	0
12	2
13	2
14	0
15	5
16	5
17	4.
18	5.
19	2.
20	2.
21	0.
22	0.
23	0.
24	0.
25	5.
26	2.
27	0.
28	5.

- This diagram is viewed from the pink colored foil side.
- This PCB is double sided.

• Waveformes at AUDIO DIGITAL BOARD ASSY

• Measuring condition : DC input unless otherwise noted.



① IC801 pin 2 (ADC LDATA)
② IC801 pin 27 (ADC RDATA)
During REC (Analog 1kHz 0dB)
1V/div 1ms/div

③ IC801 pin 14 (ADC LRCK)
④ IC801 pin 16 (ADC DATA)
⑤ IC801 pin 15 (ADC BCK)
During REC (1kHz 0dB)
10V/div 2μs/div

⑥ IC306 pin 8 (LRCK)
⑦ IC306 pin 9 (DATA)
⑧ IC306 pin 4 (BCLK)
During REC
10V/div 2μs/div

⑨ IC306 pin 26 (LRCK)
⑩ IC306 pin 25 (DATA)
⑪ IC306 pin 28 (BCLK)
During REC
10V/div 2μs/div

⑫ IC401 pin 28 (LRCK)
⑬ IC401 pin 1 (DATA)
⑭ IC401 pin 2 (BCLK)
During REC
10V/div 2μs/div

⑮ IC401 pin 26 (BCK)
⑯ IC401 pin 25 (WCK)
⑰ IC401 pin 24 (LDATA)
⑱ IC401 pin 23 (RDATA)
During PLAY
10V/div 0.5μs/div

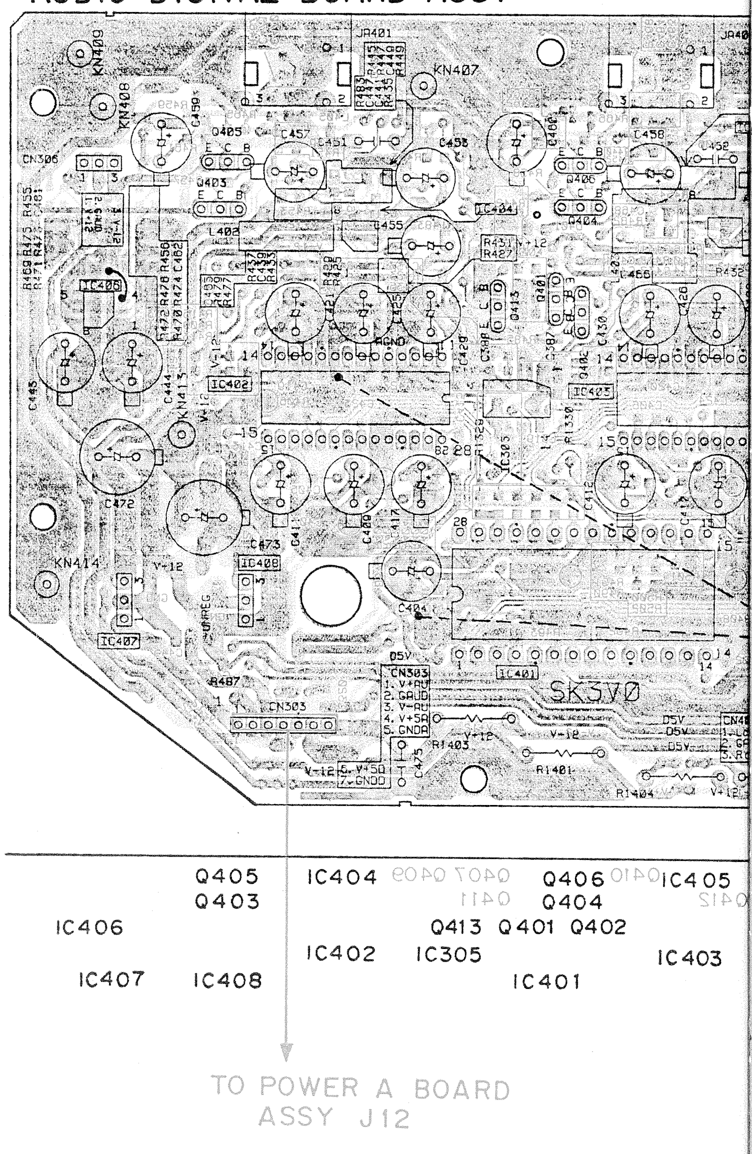
⑲ IC304 pin 9 (AO)
⑳ IC304 pin 1 (I/O)
Optical input during REC
5V/div 0.2μs/div

㉑ IC302 pin 9 (VCO IN) 1V/div
㉒ IC302 pin 4 (VCO OUT) 10V/div
㉓ IC301 pin 80 (EC ERR) 10V/div
During REC 50ns/div

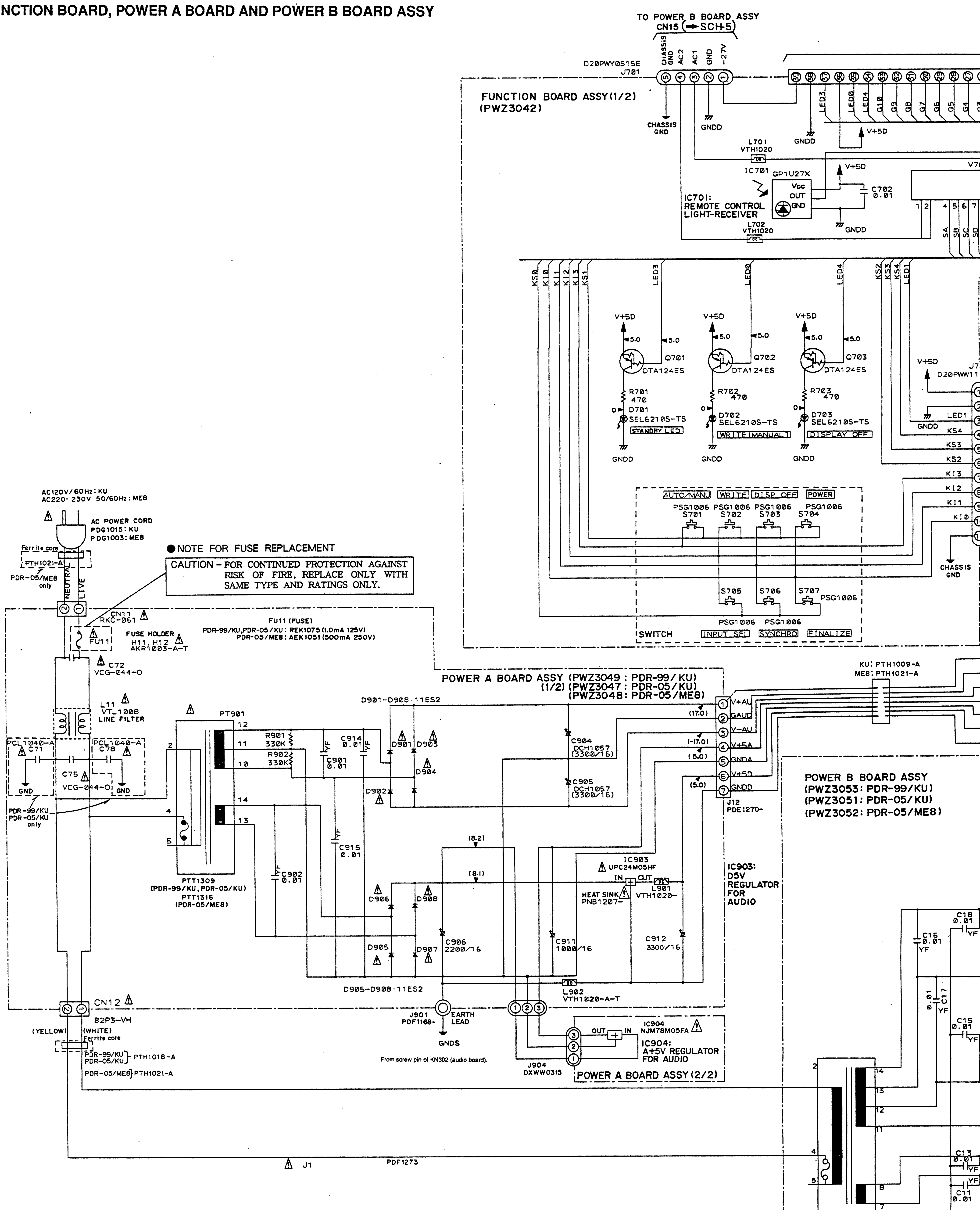
㉔ IC301 pin 1
(DIN1 : OPT IN)
㉕ IC301 pin 4
(DIN2 : COAX IN)
㉖ IC307 pin 5 (DOUT)
Optical, coaxial and simultaneous input
During REC 0.2μs/div 10V/div

㉗ IC404 pin 7 (LIN OUT Lch) 5V/div
㉘ Q407 pin emitter 5V/div
㉙ IC406 pin 7 (HP OUT Lch) 10V/div
CD 1kHz During PLAYBACK
0.5ms/div

AUDIO DIGITAL BOARD ASSY

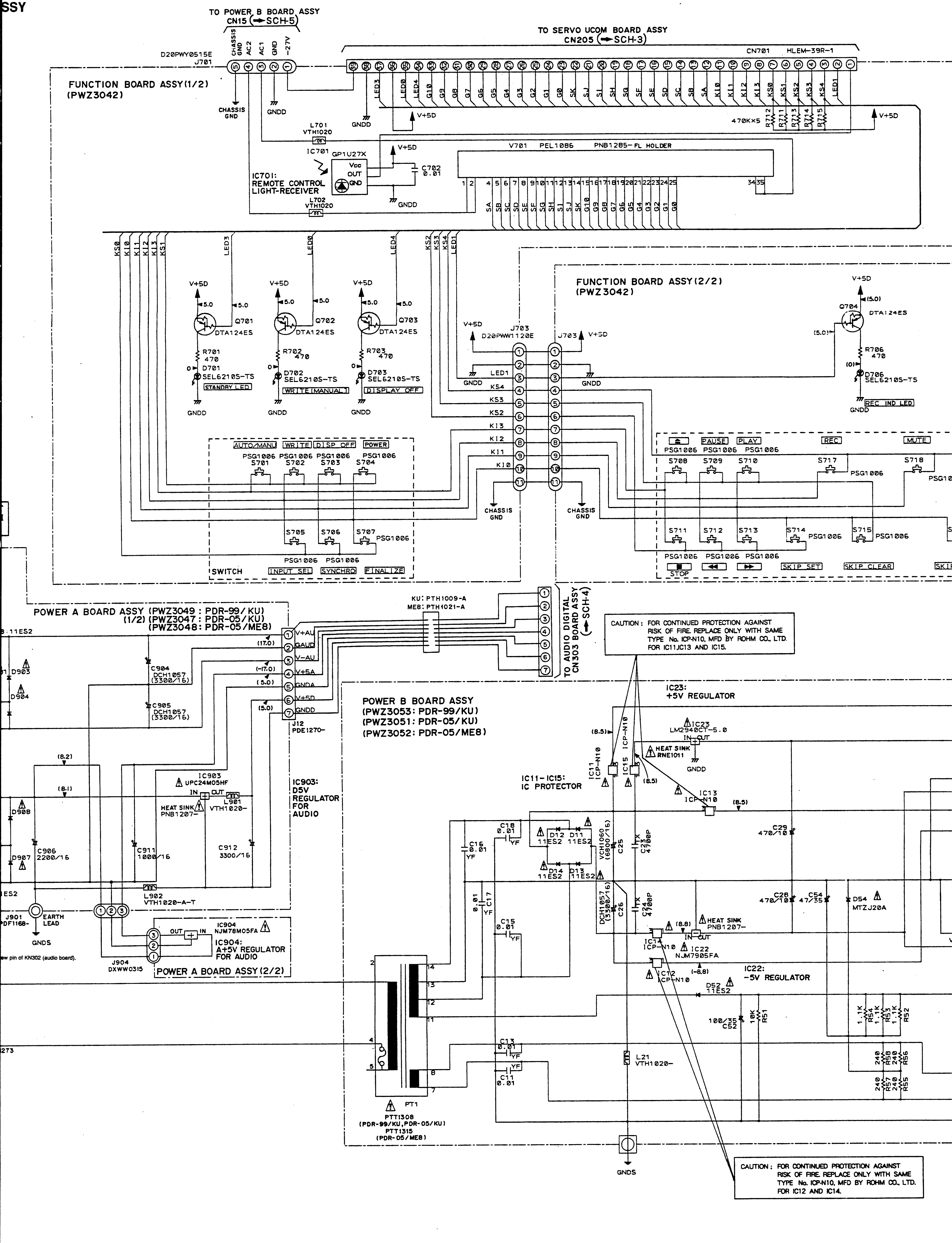


5.5 FUNCTION BOARD, POWER A BOARD AND POWER B BOARD ASSY


TO POWER B BOARD ASSY
CN15 (→SCH-5)
CHASSIS GND
AC2
AC1
GND
-27V
D20PWY0515E
J701
FUNCTION BOARD ASSY(1/2)
(PWZ3042)
CHASSIS GND
GNDD
LED3
LED0
LED4
G10
G9
G7
G6
G5
G4
V+5D
L701
VTH1020
IC701
GP1U27X
Vcc
OUT
GND
C702
0.01
IC701:
REMOTE CONTROL
LIGHT-RECEIVER
L702
VTH1020
SA
SB
SC
SD
KS0
KI0
KI1
KI2
KI3
KS1
KS2
KS3
KS4
LED1
Q701
DTA124ES
Q702
DTA124ES
Q703
DTA124ES
R701
470
R702
470
R703
470
D701
SEL6210S-TS
STANDBY LED
D702
SEL6210S-TS
WRITE MANUAL
D703
SEL6210S-TS
DISPLAY OFF
5.0
0
D20PWW11
AUTO/MANU
WRITE
DISP OFF
POWER
PSG1006
S701
S702
S703
S704
S705
S706
S707
SWITCH
INPUT SEL
SYNCHRO
FINALIZE
AC120V/60Hz: KU
AC220-230V 50/60Hz: ME8
AC POWER CORD
PDG1015: KU
PDG1003: ME8
Ferrite core
PTH1021-A
PDR-05/ME8 only
NEUTRAL
LIVE
CN11
RKC-061
FU11
FUSE HOLDER
H11, H12
AKR1003-A-T
FU11 (FUSE)
PDR-99/KU,PDR-05/KU: REK1075 (1.0mA 125V)
PDR-05/ME8: AEK1051 (500mA 250V)
C72
VCG-044-O
L11
VTL1008
LINE FILTER
PCL1040-A
C71
C78
C75
VCG-044-O
GND
PDR-99/KU, PDR-05/KU only
PT901
PTT1309
(PDR-99/KU, PDR-05/KU)
PTT1316
(PDR-05/ME8)
POWER A BOARD ASSY (PWZ3049: PDR-99/KU)
(1/2) (PWZ3047: PDR-05/KU)
(PWZ3048: PDR-05/ME8)
D901-D908: 11ES2
R901
330K
R902
330K
C914
0.01
C901
0.01
C915
0.01
C902
0.01
YF
D901
D902
D903
D904
D905
D906
D907
D908
C904
DCH1057
(3300/16)
C905
DCH1057
(3300/16)
(17.0)
(-17.0)
(5.0)
V+AU
GAUD
V-AU
V+5A
GNDA
V+5D
GNDD
J12
PDE1270-
KU: PTH1009-A
ME8: PTH1021-A
(8.2)
(8.1)
IC903
UPC24M05HF
IN
OUT
HEAT SINK
PNB1207-
L901
VTH1020-
IC903:
D5V
REGULATOR
FOR
AUDIO
C906
2200/16
C911
1000/16
C912
3300/16
D905-D908: 11ES2
L902
VTH1020-A-T
CN12
B2P3-VH
(YELLOW)
(WHITE)
Ferrite core
PDR-99/KU
PDR-05/KU
PTH1018-A
PDR-05/ME8 PTH1021-A
J901
PDF1168-
EARTH LEAD
GNDS
From screw pin of KN302 (audio board).
J904
DXWW0315
IC904
NJM78M05FA
OUT
IN
IC904:
A+5V REGULATOR
FOR AUDIO
POWER A BOARD ASSY (2/2)
J1
PDF1273
POWER B BOARD ASSY
(PWZ3053: PDR-99/KU)
(PWZ3051: PDR-05/KU)
(PWZ3052: PDR-05/ME8)
C18
0.01
C16
0.01
C17
0.01
C15
0.01
C13
0.01
C11
0.01
YF
PT1
PTT1308
(PDR-99/KU, PDR-05/KU)
PTT1315
(PDR-05/ME8)

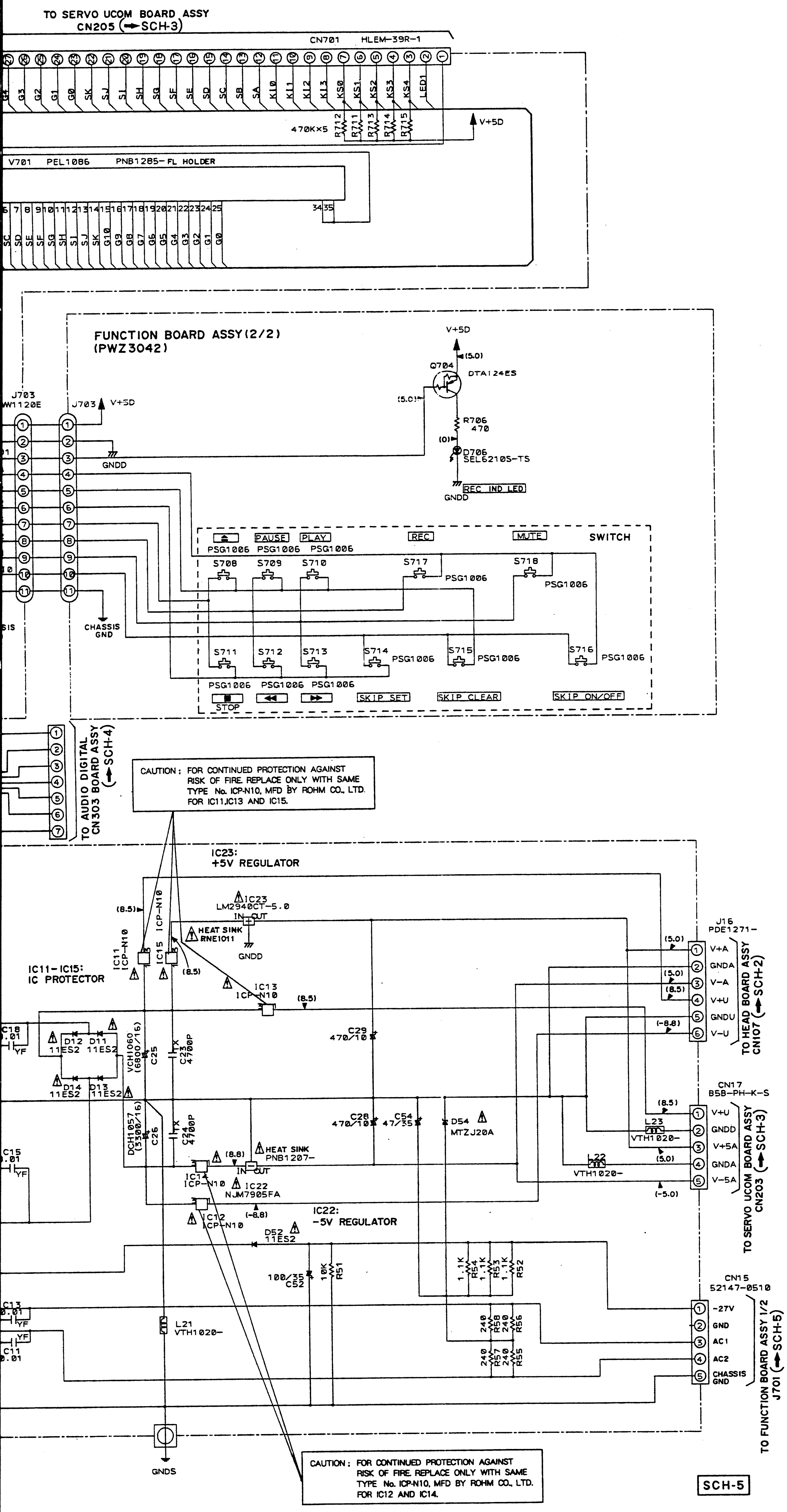
● NOTE FOR FUSE REPLACEMENT

CAUTION – FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ONLY WITH SAME TYPE AND RATINGS ONLY.


SSY
TO POWER B BOARD ASSY CN15 (➡SCH-5)
TO SERVO UCOM BOARD ASSY CN205 (➡SCH-3)
CN701 HLEM-39R-1
D20PWY0515E J701
CHASSIS GND
AC2
AC1
GND
-27V
FUNCTION BOARD ASSY(1/2) (PWZ3042)
GNDD
V+5D
470K×5
R712 R711 R713 R714 R715
L701 VTH1020
IC701 GP1U27X
Vcc OUT GND
C702 0.01
IC701: REMOTE CONTROL LIGHT-RECEIVER
L702 VTH1020
V701 PEL1086 PNB1285- FL HOLDER
LED3 LED0 LED4 G10 G9 G8 G7 G6 G5 G4 G3 G2 G1 G0 SK SJ SI SH SG SF SE SD SC SB SA K10 K11 K12 K13 KS0 KS1 KS2 KS3 KS4 LED1
Q701 DTA124ES
Q702 DTA124ES
Q703 DTA124ES
R701 470
R702 470
R703 470
D701 SEL6210S-TS
D702 SEL6210S-TS
D703 SEL6210S-TS
STANDBY LED
WRITE(MANUAL)
DISPLAY OFF
AUTO/MANU WRITE DISP OFF POWER
PSG1006
S701 S702 S703 S704
S705 S706 S707
SWITCH
INPUT SEL SYNCHRO FINALIZE
J703 D20PWW1120E
CHASSIS GND
FUNCTION BOARD ASSY(2/2) (PWZ3042)
Q704 DTA124ES
R706 470
D706 SEL6210S-TS
REC IND LED
PAUSE PLAY REC MUTE
S708 S709 S710 S717 S718
S711 S712 S713 S714 S715
STOP
SKIP SET SKIP CLEAR
POWER A BOARD ASSY (PWZ3049 : PDR-99/KU) (1/2) (PWZ3047 : PDR-05/KU) (PWZ3048: PDR-05/ME8)
KU: PTH1009-A
ME8: PTH1021-A
TO AUDIO DIGITAL BOARD ASSY CN303 (➡SCH-4)
V+AU GAUD V-AU V+5A GNDA V+5D GNDD
J12 PDE1270-
C904 DCH1057 (3300/16)
C905 DCH1057 (3300/16)
D903 D904 D908 D907
IC903 UPC24M05HF
HEAT SINK PNB1207-
L901 VTH1020-
IC903: D5V REGULATOR FOR AUDIO
C906 2200/16
C911 1000/16
C912 3300/16
L902 VTH1020-A-T
J901 PDF1168-
EARTH LEAD
GNDS
IC904 NJM78M05FA
IC904: A+5V REGULATOR FOR AUDIO
J904 DXWW0315
POWER A BOARD ASSY(2/2)
ew pin of KN302 (audio board).
POWER B BOARD ASSY (PWZ3053: PDR-99/KU) (PWZ3051: PDR-05/KU) (PWZ3052: PDR-05/ME8)
IC23: +5V REGULATOR
IC23 LM2940CT-5.0
HEAT SINK RNE1011
IC11-IC15: IC PROTECTOR
IC11 ICP-N10
IC15 ICP-N10
IC13 ICP-N10
C18 0.01
C16 0.01
D12 D11 11ES2
D14 D13 11ES2
VCH1060 (6800/16)
C25
C23 4700P
C29 470/10
C17 0.01
C15 0.01
DCH1057 (3300/16)
C26
C24 4700P
C28 470/10
C54 47/35
D54 MTZJ20A
HEAT SINK PNB1207-
IC14 ICP-N10
IC22 NJM7905FA
IC12 ICP-N10
IC22: -5V REGULATOR
D52 11ES2
C52 100/35
R51 10K
R54 1.1K R53 1.1K R52
R58 240 R56 240
R57 240 R55 240
C13 0.01
C11 0.01
L21 VTH1020-
PT1 PTT1308 (PDR-99/KU, PDR-05/KU) PTT1315 (PDR-05/ME8)
GNDS

CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE REPLACE ONLY WITH SAME TYPE No. ICP-N10, MFD BY ROHM CO., LTD. FOR IC11,IC13 AND IC15.

CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE REPLACE ONLY WITH SAME TYPE No. ICP-N10, MFD BY ROHM CO., LTD. FOR IC12 AND IC14.



TO SERVO UCOM BOARD ASSY
CN205 (→SCH-3)
CN701 HLEM-39R-1
G4 G3 G2 G1 G0 SK SJ SI SH SG SF SE SD SC SB SA KI0 KI1 KI2 KI3 KS0 KS1 KS2 KS3 KS4 LED1
470K×5
R712 R711 R713 R714 R715
V+5D
V701 PEL1086 PNB1285-FL HOLDER
SC SD SE SF SG SH SI SJ SK G10 G9 G8 G7 G6 G5 G4 G3 G2 G1 G0
FUNCTION BOARD ASSY(2/2)
(PWZ3042)
V+5D
(5.0)
Q704
DTA124ES
(5.0)
R706
470
(0)
D706
SEL6210S-TS
REC IND LED
GNDD
J703
W1120E
J703
V+5D
GNDD
CHASSIS GND
SWITCH
PAUSE
PLAY
REC
MUTE
PSG1006
S708 S709 S710 S717 S718
S711 S712 S713 S714 S715 S716
STOP
SKIP SET
SKIP CLEAR
SKIP ON/OFF
TO AUDIO DIGITAL BOARD ASSY
CN303 (→SCH-4)
IC23:
+5V REGULATOR
IC23
LM2940CT-5.0
IN OUT
HEAT SINK
RNE1011
GNDD
(8.5)
IC11 ICP-N10
IC15 ICP-N10
IC11-IC15:
IC PROTECTOR
IC13
ICP-N10
(8.5)
C18
.01
YF
D12 D11
11ES2 11ES2
D14 D13
11ES2 11ES2
VCH1060
(6800/16)
C25
C23
4700P
C29
470/10
DCH1057
(3300/16)
C26
C24
4700P
C28
470/10
C54
47/35
D54
MTZJ20A
C15
.01
YF
(8.8)
HEAT SINK
PNB1207-
IC14
ICP-N10
IC22
NJM7905FA
IC12
ICP-N10
(-8.8)
IC22:
-5V REGULATOR
D52
11ES2
100/35
C52
10K
R51
1.1K R54
1.1K R53
1.1K R52
240 R58
240 R56
240 R57
240 R55
C13
.01
YF
C11
.01
L21
VTH1020-
GNDS
J16
PDE1271-
(5.0)
V+A
GNDA
(5.0)
V-A
(8.5)
V+U
GNDU
(-8.8)
V-U
TO HEAD BOARD ASSY
CN107 (→SCH-2)
CN17
B5B-PH-K-S
(8.5)
V+U
L23
GNDD
VTH1020-
V+5A
L22
(5.0)
GNDA
VTH1020-
V-5A
(-5.0)
TO SERVO UCOM BOARD ASSY
CN203 (→SCH-3)
CN15
52147-0510
-27V
GND
AC1
AC2
CHASSIS GND
TO FUNCTION BOARD ASSY 1/2
J701 (→SCH-5)
SCH-5

CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE REPLACE ONLY WITH SAME TYPE No. ICP-N10, MFD BY ROHM CO., LTD. FOR IC11,IC13 AND IC15.

CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE REPLACE ONLY WITH SAME TYPE No. ICP-N10, MFD BY ROHM CO., LTD. FOR IC12 AND IC14.

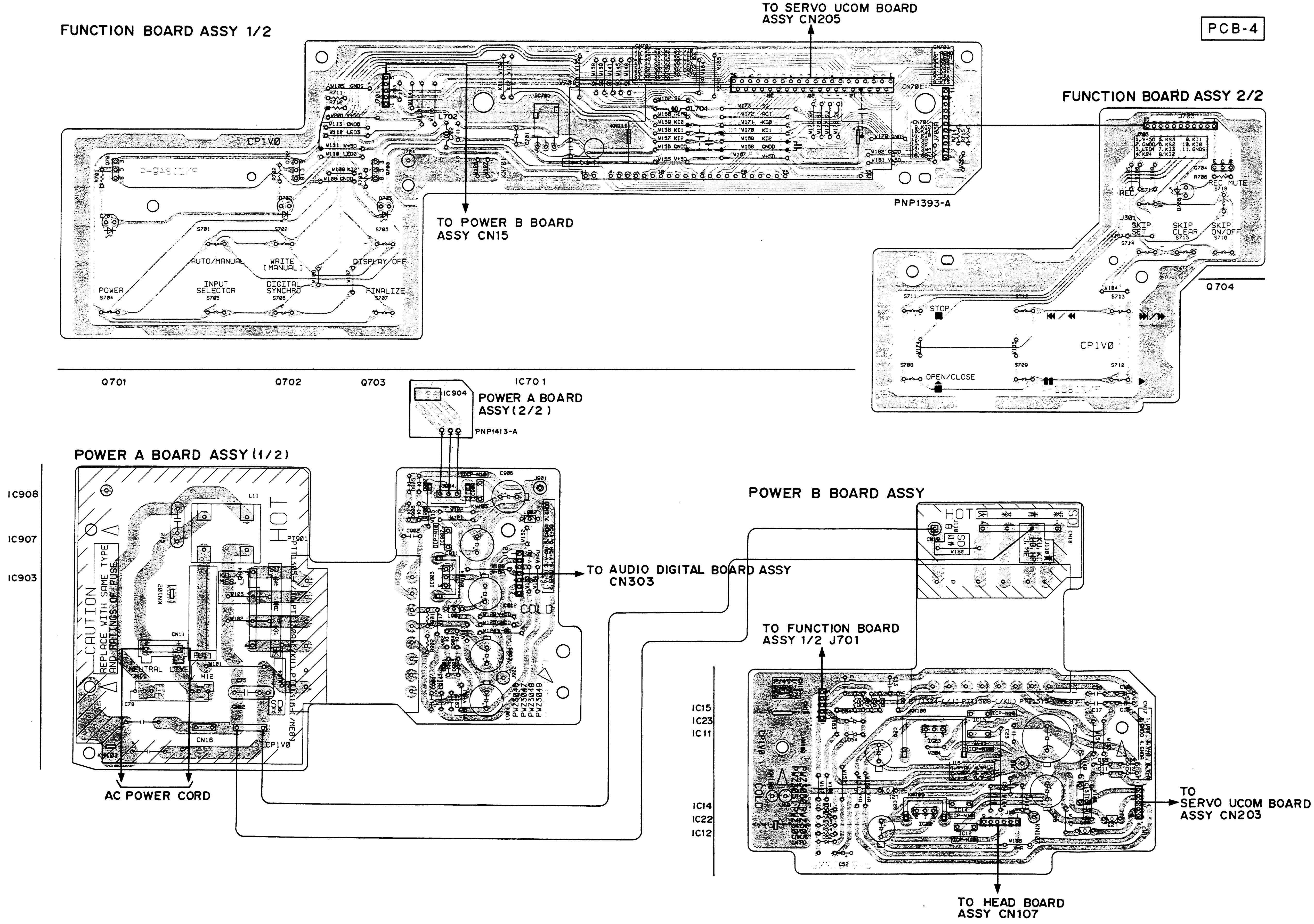
FUNCTION BOARD ASSY,
POWER A BOARD ASSY,
POWER B BOARD ASSY

SCH-5

- **This diagram is viewed from the mounted parts side.**

- The parts mounted on this PCB include all necessary parts for several destinations.
For further information for respective destinations, be sure to check with the schematic diagram.

PCB-4


FUNCTION BOARD ASSY 1/2
TO SERVO UCOM BOARD ASSY CN205
FUNCTION BOARD ASSY 2/2
CN701
CP1V0
POWER S704
INPUT SELECTOR S705
AUTO/MANUAL S701
WRITE [MANUAL] S702
DIGITAL SYNCHRO S706
DISPLAY OFF S703
FINALIZE S707
TO POWER B BOARD ASSY CN15
PNP1393-A
REC
REC MUTE S718
SKIP SET S714
SKIP CLEAR S715
SKIP ON/OFF S716
STOP S711
OPEN/CLOSE S708
S712
S713
S709
S710
Q704
Q701
Q702
Q703
IC701
IC904
POWER A BOARD ASSY (2/2)
PNP1413-A
POWER A BOARD ASSY (1/2)
IC908
IC907
IC903
CAUTION
REPLACE WITH SAME TYPE AND RATINGS OF FUSE
HOT
COLD
NEUTRAL
LIVE
CN11
CN16
AC POWER CORD
TO AUDIO DIGITAL BOARD ASSY CN303
POWER B BOARD ASSY
HOT
SD
TO FUNCTION BOARD ASSY 1/2 J701
IC15
IC23
IC11
IC14
IC22
IC12
TO SERVO UCOM BOARD ASSY CN203
TO HEAD BOARD ASSY CN107

6. PCB PARTS LIST

NOTES:

- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by " ⊙ " are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*
- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

Ex.1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47K ohm (tolerance is shown by J=5%, and K=10%).

560 Ω → 56 × 10^1 → 561 .... RD1/8PM 561 J
47 kΩ → 47 × 10^3 → 473 .... RD1/4PS 473 J
0.5 Ω → 0R5 .... RN2H 0R5 K
1 Ω → 010 .... RS1P 010 K

Ex.2 When there are 3 effective digits (such as in high precision metal film resistors).

5.62 kΩ → 562 × 10^1 → 5621 .... RN1/4PC 5621 F

■ LIST OF WHOLE PCB ASSEMBLIES

Mark	PCB Assemblies	Part No.			RemarKs
		PDR-99/KU	PDR-05/KU	PDR-05/ME8	
	MOTHER BOARD ASSY	PWM1973	PWM1971	PWM1972	
	├ HEAD BOARD ASSY	PWZ3022	PWZ3022	PWZ3022	
	├ SERVO UCOM BOARD ASSY	PWZ3027	PWZ3029	PWZ3028	
	├ AUDIO DIGITAL BOARD ASSY	PWZ3033	PWZ3031	PWZ3032	
NSP	├ REC VR BOARD ASSY	PWZ3034	PWZ3034	PWZ3034	
NSP	├ H. P BOARD ASSY	PWZ3038	PWZ3038	PWZ3038	
NSP	└ MECHANISM BOARD ASSY	PWZ3062	PWZ3062	PWZ3062	
NSP	FRONT BOARD ASSY	PWX1416	PWX1414	PWX1415	
	├ FUNCTION BOARD ASSY	PWZ3042	PWZ3042	PWZ3042	
	├ POWER A BOARD ASSY	PWZ3049	PWZ3047	PWZ3048	
	└ POWER B BOARD ASSY	PWZ3053	PWZ3051	PWZ3052	

■ CONTRAST OF PCB ASSEMBLIES

SERVO UCOM BOARD ASSY

PWZ3027, PWZ3029 and PWZ3028 have the same construction except for the following:

Mark	Symbol & Description	Part No.			RemarKs
		PWZ3027	PWZ3029	PWZ3028	
	IC352	LC3517BML-15	LH5116NA-10	LC3517BML-15	
	C5001	Not Used	Not Used	CQMA104J50	
	J221	Not Used	Not Used	XDF-535	
	R5050	RS1/10S000J	RS1/10S000J	Not Used	
	S201	PSH1010	Not Used	PSH1010	

POWER A BOARD ASSY

PWZ3049, PWZ3047 and PWZ3048 have the same construction except for the following:

Mark	Symbol & Description	Part No.			RemarKs
		PWZ3049	PWZ3047	PWZ3048	
	C906	PCH1121*	CEAS222M16	PCH1121*	*2200 μF16V
	C911	PCH1122*	CEAS102M16	PCH1122*	*1000 μF16V

POWER B BOARD ASSY

PWZ3053, PWZ3051 and PWZ3052 have the same construction except for the following:

Mark	Symbol & Description	Part No.			RemarKs
		PWZ3053	PWZ3051	PWZ3052	
	C28, C29	VCH1116*	CEAS471M10	VCH1116*	*470 μF/10V
	C52	PCH1126*	CEAS101M35	PCH1126*	*2200 μF/25V
	C54	PCH1124*	CEAS470M35	PCH1124*	*47 μF/50V

AUDIO DIGITAL BOARD ASSY

PWZ3033, PWZ3031 and PWZ3032 have the same construction except for the following:

Mark	Symbol & Description	Part No.			RemarKs
		PWZ3033	PWZ3031	PWZ3032	
	IC401	PD7009A	SM5813AP	PD7009A	
	IC402, IC403	PD2028B(S)	PD2028B	PD2028B(S)	
	C404, C409–C412, C417, C418, C421, C425, C426, C430	VCH1116*	CEAS471M6R3	VCH1116*	*470 μF/16V
	C443, C444	CEZA470M16	CEAS470M16	CEZA470M16	
	C451, C452	CFTXA102J50	CKSQYB102K50	CFTXA102J50	
	C457, C458, C805, C806, C811–C814, C842–C844, C848	CEZA220M50	CEAS220M50	CEZA220M50	
	C459, C460, C832	CEZA4R7M50	CEAS4R7M50	CEZA4R7M50	
	C472, C473	PCH1122*	CEAS222M16	PCH1122*	*1000 μF/16V
	C817, C818, C833, C835	CEZA100M50	CEAS100M50	CEZA100M50	
	R490, R502	RS1/10S000J	Not Used	RS1/10S000J	
	R492, R493	Not Used	RS1/10S000J	Not Used	

■ PARTS LIST FOR PDR-99/KU

HEAD BOARD ASSY

SEMICONDUCTORS

Mark	No.	Description	Parts No.
	IC102, IC104		BA4560F
⚠	IC202		LA6517
⚠	IC203		LA6520
	IC101		PA4022A
	IC103		TC7S08F
	Q103-Q106		2SA1037K
	Q107, Q108		2SA1461
	Q102		2SB1189
	Q101		2SC2412K
	Q110		2SJ146
	Q115		DTA114EK
	Q111		DTA114TK
	Q117		DTA124EK
	Q116		DTC114TK
	Q109		DTC114TS
	Q113		DTC144ES
	D101		DA114
	D110		DTZJ6.2B

CAPACITORS

Mark	No.	Description	Parts No.
	C140		CCSQCH020C50
	C103, C142, C145, C146		CCSQCH100D50
	C143		CCSQCH220J50
	C123, C124		CCSQCH221J50
	C109-C112		CCSQCH391J50
	C147, C148		CCSQCH471J50
	C122		CCSQCH620J50
	C105-C108		CCSQSL821J50
	C116		CEJA100M16
	C101, C102, C113, C121, C125		CEJA101M10
	C221, C224, C227, C230		CEJA470M16
	C117		CEJANP2R2M35
	C127		CEJANP4R7M16
	C133		CFTXA103J50
	C114, C130, C131, C137, C138		CKSQYB103K50
	C141		CKSQYB103K50
	C128		CKSQYB182K50
	C11		CKSQYB683K25
	C104, C118, C120, C126		CKSQYF103Z50
	C134, C135, C139, C164, C189		CKSQYF103Z50
	C220, C222, C223, C225, C226		CKSQYF103Z50
	C228, C229, C232		CKSQYF103Z50
	C115, C132		CKSQYF104Z25
	C9		CKSRYB392K50
	C144		CKSRYF103Z50

RESISTORS

Mark	No.	Description	Parts No.
	R130 (62Ω)		PCN1037
	R148 (2.2kΩ)		PCN1038
	R1104 (2.2kΩ)		PCN1039
	R138, R162		RN1/10SE123D
	R136, R161		RN1/10SE303D
	R1105		RS1/16S222J
	R2		RS1/16S104J
	R135		RS1/16S132J
	R6		RS1/16S133J
	R134		RS1/16S362J
	R12		RS1/16S471J
	R1106		RS1/16S202J
	R8		RS1/16S472J
	VR10 (2.2kΩ)		RCP1019
	VR1, VR103-VR105, VR107, VR108 (10kΩ)		RCP1045
	VR112, VR115 (10kΩ)		RCP1045
	VR106, VR110, VR111 (22kΩ)		RCP1046
	VR119 (47kΩ)		RCP1047
	Other Resistors		RS1/10S□□□J

OTHERS

Mark	No.	Description	Parts No.
	CN106	ZH CONNECTOR 10P	S10B-ZR
	CN105	ZH CONNECTOR 13P	S13B-ZR
	CN107	KR CONNECTOR	S6B-PH-K-S
		PCB BINDER	VEF1008

SERVO UCOM BOARD ASSY

Note:
* 1: Ask PIONNER subsidiaries/distributors if these parts are to be replaced or repaired.

SEMICONDUCTORS

Mark	No.	Description	Parts No.
	IC5008		BA4560F
	IC360		* 1
	IC201		CXA1372Q
	IC206		CXD2500BQ
	IC204, IC5024		HD74HC4053FP
	IC353		HD74HC573FP
	IC352		LC3517BML-15
⚠	IC208		LM2940CT-5.0
	IC205		PA9004A
	IC356		PD4584A
	IC351		PD4591A
	IC207		PDJ006A
	IC311		PST529C
	IC361		PST572E
	IC357, IC358		TC74HC367AF
	IC354		TC7S00F
	IC355, IC359, IC362		TC7S04F
	IC363		TC7S14F
	Q203		2SA1037K
	Q202		2SC2412K
	Q14		DTA124EK
	Q201, Q5026		DTA124ES
	Q13		DTC114TK
	Q208		DTC114TS
	D219-D222, D353		1SS133

Mark	No.	Description	Parts No.
	D354		DA114
	D206		DA204K
	D1351		DAN202K
	D210		DAP202K
	D202, D205		MTZJ3.9BX

COILS AND FILTERS

	L201		PTL1014

SWITCHES AND RELAYS

	S201		PSH1010

CAPACITORS

	C291		CCSQCH100D50
	C1221, C1308, C284, C295, C298		CCSQCH101J50
	C247-C257		CCSQCH121J50
	C355, C356		CCSQCH150J50
	C282		CCSRCH101J50
	C12		CCSRCH270J50
	C278		CEAS010M50
	C241		CEAS100M50
	C209, C212, C290		CEAS101M6R3
	C1302, C264, C271		CEAS2R2M50
	C205, C235-C238, C293, C5016		CEAS470M10
	C5018		CEAS470M10
	C240		CEAS471M10
	C351, C358		CEAS471M6R3
	C203, C207		CEAS4R7M50
	C288		CEASR47M50
	C201, C202, C204, C206, C274, C1310		CKSQYB104K25
	C5004		CKSQYB222K50
	C1309		CKSQYB272K50
	C5013		CKSQYB333K50
	C1304, C5005-C5008		CKSQYB471K50
	C260		CKSQYB683K25
	C233, C234, C239, C242, C280		CKSQYF103Z50
	C5017, C5019		CKSQYF103Z50
	C1301, C1307, C285, C292, C352		CKSQYF104Z25
	C357		CKSQYF104Z25
	C283, C294		CKSQYF473Z50
	C279		CKSRYB102K50
	C208, C210, C213, C218, C289		CKSRYB103K50
	C287		CKSRYB152K50
	C258		CKSRYB223K25
	C267-C270		CKSRYB331K50
	C219, C262		CKSRYB332K50
	C211, C217		CKSRYB333K16
	C214, C215		CKSRYB472K50
	C216, C261, C286		CKSRYB473K16
	C259		CKSRYB681K50
	C1202, C353, C354, C360, C370		CKSRYF103Z50
	C1305, C1306, C359		CKSRYF104Z25
	C281		CKSRYF473Z25
	C272, C273		CQMA104J50
	C361 (0.22 μF/5.5V)		PCH1131
	C263, C275-C277 (0.33 μF/16V)		PCL1043
	C5002, C5011 (0.15 μF/16V)		PCL1044

Mark	No.	Description	Parts No.
	C1201 (0.082 μF/16V)		PCL1045
	C243 (0.1 μF/16V)		PCL1046

RESISTORS

	R1, R1211, R1212, R1214		RS1/16S000J
	R1381-R1388		RS1/16S101J
	R233, R5007		RS1/16S102J
	R1308, R213, R214, R216		RS1/16S103J
	R247, R248, R256-R259, R266		RS1/16S103J
	R268, R5006, R1215		RS1/16S103J
	R251, R260, R267		RS1/16S104J
	R206, R241		RS1/16S105J
	R253, R254		RS1/16S114J
	R5030		RS1/16S123J
	R353-R361		RS1/16S124J
	R208, R232		RS1/16S133J
	R201		RS1/16S184J
	R210		RS1/16S204J
	R5022		RS1/16S221J
	R5023		RS1/16S222J
	R1202, R1204, R234, R236		RS1/16S273J
	R203, R212		RS1/16S274J
	R211, R242		RS1/16S302J
	R270		RS1/16S332J
	R252		RS1/16S333J
	R243		RS1/16S362J
	R1206		RS1/16S393J
	R215, R217		RS1/16S470J
	R1205, R218		RS1/16S472J
	R1351-R1354, R1356-R1358, R1360		RS1/16S473J
	R246, R373, R377, R379-R383		RS1/16S473J
	R389-R391, R393-R399		RS1/16S473J
	R249		RS1/16S474J
	R235, R237		RS1/16S512J
	R209		RS1/16S514J
	R238		RS1/16S562J
	R255		RS1/16S563J
	R269		RS1/16S682J
	R202, R204		RS1/16S683J
	R250		RS1/16S684J
	R205		RS1/16S754J
	R207		RS1/16S823J
	R5025		RS1/16S912J
	VR201, VR202 (10kΩ)		RCP1045
	Other Resistors		RS1/10S□□□J

OTHERS

	CN202	5P MT CONNECTOR	173981-5
	CN211	3P JUMPER CONNECTOR	52147-0310
	CN5021	3P TOP POST	B3P-SHF-1AA
	CN203	KR CONNECTOR	B5B-PH-K-S
	CN204	6P TOP POST	B6P-SHF-1AA
	CN206	5P SIDE POST	BS5P-SHF-1AA
	CN205	39P FFC CONNECTOR	HLEM39S-1
	J201	13P CONNECTOR ASSY	PDE1264

Mark	No.	Description	Parts No.
	J210	10P CONNECTOR ASSY	PDE1269
	JA201, JA202	JACK/12V	PKN1004
	X352	CERAMIC RESONATOR (16.00MHz)	PSS1010
		PCB BINDER	VEF1008
	X351	CERAMIC RESONATOR (4.19MHz)	VSS1014

AUDIO DIGITAL BOARD ASSY

SEMICONDUCTORS

Mark	No.	Description	Parts No.
	IC801		AK5340-VS
	IC302		CD74HC4046AM
	IC406		M5218AFP
	IC304		MB81C4256A-80LPJ
	IC803, IC804		NJM4580D
	IC404, IC405		NJM5532MD
⚠	IC407		NJM7812FA
⚠	IC408		NJM7912FA
	IC303		PCX1021
	IC402, IC403		PD2028B(S)
	IC401		PD7009A
	IC301		PDC019A
	IC306		PDC020A
	IC309, IC310		TC74HC00AF
	IC307, IC308		TC74HCU04AF
	IC312		TC7S14F
	Q407-Q412		2SD2114K
	Q301, Q303		DTA114TS
	Q402-Q404, Q413		DTA124ES
	Q304		DTC114EK
	Q302		DTC124EK
	Q401, Q405, Q406		DTC124ES
	D302		1SR35-100AVL
	D402, D403		DA114
	D301		DA204K
	D801, D803		DAN202K
	D401, D802, D804		DAP202K

COILS AND FILTERS

Mark	No.	Description	Parts No.
	L831, L832		LFA010K
	L318		PTL1003
	L301-L306, L308-L314		PTL1014
	L316, L317, L319, L328, L329		PTL1014
	L401-L406		PTL1014
	L321	(80μH)	PTL1017
	L320	EMI FILTER	PTL1019
	L330	EMI FILTER	PTL1020

CAPACITORS

Mark	No.	Description	Parts No.
	C1332		CCSQCH100D50
	C321, C368, C369, C381, C383		CCSQCH101J50
	C401, C463, C470, C477, C478		CCSQCH101J50
	C801, C821		CCSQCH101J50
	C803, C804		CCSQCH121J50
	C431, C432, C435, C436		CCSQCH181J50
	C433, C434, C437, C438		CCSQCH330J50
	C365, C378, C380, C439-C442		CCSQCH470J50
	C449, C450		CCSQCH681J50
	C319, C382		CCSRCH101J50
	C308		CCSRCH120J50
	C330		CCSRCH180J50
	C309		CCSRCH270J50
	C339, C341, C366		CEAS100M16
	C302, C306, C310, C314, C324		CEAS101M6R3
	C333, C337, C377		CEAS101M6R3
	C453-C456		CEAS221M25
	C362		CEAS330M35
	C315, C323, C328, C331, C343		CEAS470M10
	C817, C818, C833, C835		CEZA100M50
	C457, C458, C805, C806		CEZA220M50
	C811-C814, C842-C844, C848		CEZA220M50
	C443, C444		CEZA470M16
	C459, C460, C832		CEZA4R7M50
	C451, C452		CFTXA102J50
	C317, C329		CFTXA105J50
	C345, C347		CKCYB101K50
	C475		CKCYB103K50
	C346, C348, C363, C823		CKCYF473Z50
	C845		CKSQYB102K50
	C326, C385, C387, C405, C406		CKSQYB103K50
	C336, C407, C408, C419, C420		CKSQYB104K25
	C423, C424		CKSQYB104K25
	C427, C428, C390		CKSQYB472K50
	C303, C307, C402, C403		CKSQYB473K25
	C447, C448		CKSQYB562K50
	C465, C466		CKSQYB683K25
	C819, C820		CKSQYB821K50
	C413-C416		CKSQYB822K50
	C1331, C445, C446, C467, C468		CKSQYF103Z50
	C807-C810, C846		CKSQYF103Z50
	C311, C313, C316, C322, C325		CKSQYF104Z25
	C327, C332, C334, C338, C342		CKSQYF104Z25
	C344, C364, C367, C376, C469		CKSQYF104Z25
	C474, C815, C816, C831, C834		CKSQYF104Z25
	C836, C847		CKSQYF104Z25
	C320, C349, C350, C371-C375		CKSQYF473Z50
	C301		CKSRYB102K50
	C1333, C305, C318		CKSRYB103K50
	C312		CKSRYB472K50
	C304		CKSRYF104Z25
	C379		CQMA10[illegible]K50
	C335		CQMA10[illegible]J50
	C472, C473 (2200μF/16V)		PCH1121
	C404, C409-C412, C417, C418 (470μF/16V)		VCH1116
	C421, C425, C426 (470μF/16V)		VCH1116
	C430 (470μF/16V)		VCH1116

RESISTORS

Mark	No.	Description	Parts No.
	R3331		RS1/16S000J
	R1329, R1330, R1336, R306-R309		RS1/16S101J
	R314-R317, R323, R324, R326		RS1/16S101J
	R328, R334-R336, R341-R343		RS1/16S101J
	R300, R311, R313, R329, R331		RS1/16S102J
	R320		RS1/16S105J
	R305, R337		RS1/16S151J
	R1333		RS1/16S221J
	R1335, R444, R499		RS1/16S271J
	R498		RS1/16S331J
	R1324		RS1/16S332J
	R301, R339		RS1/16S333J
	R302		RS1/16S363J
	R344		RS1/16S470J
	R347, R348		RS1/16S472J
	R345, R349		RS1/16S473J
	R303, R304, R338, R340, R1323		RS1/16S512J
	R312, R330		RS1/16S681J
	R1401-R1404		RS1/2LMF270J
	Other Resistors		RS1/10S□□□J

OTHERS

	CN401	3P JUMPER CONNECTOR	52147-0310
	JA301	OPTICAL RECEIVER MODULE	GP1F32R
	JA303	OPTICAL TRANSMITTER MODULE	GP1F32T
	JA302	1P JACK	PKB1027
	JA304	1P JACK	PKB1028
	JA801	2P JACK	PKB1029
	JA401	1P JACK	PKB1030
	JA402	1P JACK	PKB1031
	KN302	SCREW TERMINAL	PNB1558
	X301	XTAL RESONATOR(16.9344MHz)	PSS1008
	PCB BINDER		VEF1008
	KN301	EARTH METAL FITTING	VNF1084

REC VR BOARD ASSY

RESISTORS

	VR801 (50kΩ -A)		RCV1091
	VR802 (50kΩ)		RCV1092
	Other Resistors		RS1/10S□□□J

OTHERS

	J801	7P CONNECTOR ASSY	PDE1274

H. P BOARD ASSY

COILS AND FILTERS

	L461-L463		PTL1014

CAPACITORS

	C1466-C1468		CCSQCH101J50
	C1463-C1465		CKSQYF103Z50

OTHERS

Mark	No.	Description	Parts No.
	VR401	VARIABLE RESISTOR (5kΩ -B)	PCS1003
	JA403	HEADPHONE JACK	RKN1002
		PCB BINDER	VEF1008

FUNCTION BOARD ASSY

SEMICONDUCTORS

	Q701-Q704		DTA124ES
	D701-D703, D706		SEL6210S

SWITCHES AND RELAYS

	S701-S718		PSG1006

COILS AND FILTERS

	L701		PTH1073
	L702		PTH1016

CAPACITORS

	C702		CKCYF103Z50

RESISTORS

	All Resistors		RD1/6PM□□□J

OTHERS

		REMOTE RECEIVER UNIT	GP1U27X
	CN701	39P FFC CONNECTOR	HLEM39R-1
	V701	FL INDICATOR TUBE	PEL1086

POWER A BOARD ASSY

SEMICONDUCTORS

⚠	IC903		UPC24M05HF
⚠	IC904		NJM78M05FA
⚠	D901-D908		11ES2

COILS AND FILTERS

	L901, L902		VTH1020
	L11		VTL1008

CAPACITORS

	C901, C902, C914, C915		CKCYF103Z50
	C904, C905, C912 (3300 μ F/16V)		DCH1057
	C906 (2200 μ F/16V)		PCH1121
	C911 (1000 μ F/16V)		PCH1122
⚠	C71, C78 (100PF/400VAC)		PCL1040
⚠	C72, C75 (0.01UF/400VAC)		VCG-044

RESISTORS

	All Resistors		RD1/6PM□□□J

OTHERS

⚠	H11, H12	FUSE HOLDER	AKR1003
⚠	CN12	2P-VH CONNECTOR	B2P3-VH
	J12	7P CONNECTOR ASSY	PDE1270
	J901	EARTH LEAD UNIT	PDF1168
⚠	CN11	TERMINAL	RKC-061
		PCB BINDER	VEF1040

POWER B BOARD ASSY

SEMICONDUCTORS

Mark	No.	Description	Parts No.
⚠	IC11-IC15		ICP-N10
⚠	IC23		LM2940CT-5.0
⚠	IC22		NJM7905FA
⚠	D11-D14, D52		11ES2
⚠	D54		MTZJ20A

COILS AND FILTERS

Mark	No.	Description	Parts No.
	L21-L23		VTH1020

CAPACITORS

Mark	No.	Description	Parts No.
	C23, C24		CFTXA472J50
	C11, C13, C15-C18		CKCYF103Z50
	C26 (3300 μF/16V)		DCH1057
	C54 (47 μF/50V)		PCH1124
	C52 (100 μF/50V)		PCH1126
	C25 (6800 μF/16V)		VCH1060
	C28, C29 (2200 μF/25V)		VCH1116

RESISTORS

Mark	No.	Description	Parts No.
	All Resistors		RD1/6PM□□□J

OTHERS

Mark	No.	Description	Parts No.
	CN15	5P JUMPER CONNECTOR	52147-0510
	CN17	KR CONNECTOR	B5B-PH-K-S
	J16	6P CONNECTOR ASSY	PDE1271
		PCB BINDER	VEF1008
		EARTH METAL FITTING	VNF-091

MECHANISM BOARD ASSY

SEMICONDUCTORS

Mark	No.	Description	Parts No.
	D1001		GP1S24
	PC1001		NJL5803K-F1

RESISTORS

Mark	No.	Description	Parts No.
	All Resistors		RS1/10S□□□J

OTHERS

Mark	No.	Description	Parts No.
	J1002	7P CONNECTOR ASSY	PDE1260

7. ADJUSTMENTS

1. Adjustment Methods

If a compact disc recorder is adjusted incorrectly or inadequately, it may malfunction or not work at all even though there is nothing at all wrong with the pickup or the circuitry. Adjust correctly following the adjustment procedure.

● Measuring Instruments and Tools

1. Dual trace oscilloscope (10 : 1 probe)
2. Low-frequency oscillator
3. Test disc (STD-903), (STD-R03)
4. Low pass filter (15kΩ + 0.001μF), (39kΩ + 0.001μF)
5. Hi pass filter (3.9kΩ + 180PF)
6. Resistor (100kΩ)
7. Hexagonal screwdriver (1.27mm diagonal)
8. Standard tools
9. Small screwdriver
10. Multimeter (Voltage accuracy:Below 1 mV)

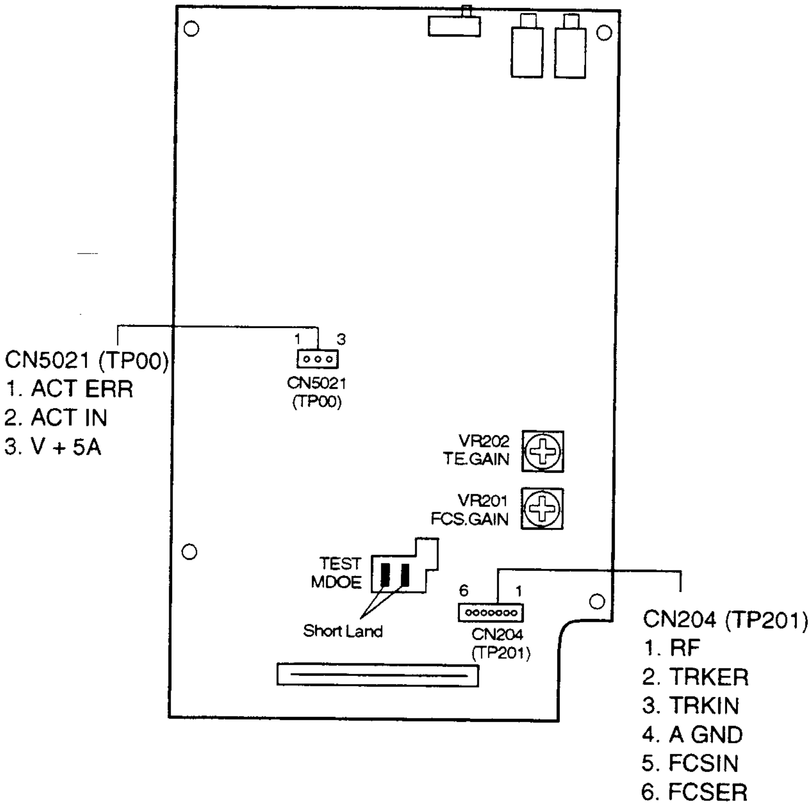
● Adjustment Items/Verification Items and Order

Adjustment 1

Step	Item	Test Point	Adjustment Location
1	Playback power adjustment	CN104 (TP1), Pin7 (PWAJT)	VR103 (PB. PW)
2	Coarse focus offset adjustment	CN204 (TP201), Pin1 (RF)	VR105 (FE, OFS)
3	Coarse skew adjustment	CN204 (TP201), Pin1 (RF)	Radial tilt adjustment screw and Tangential tilt adjustment screw
4	Coarse grating adjustment	CN104 (TP1), Pin3 (TE)	Grating adjustment slit
5	DPP (tracking offset) adjustment	CN104 (TP1), Pin3 (TE)	VR112 (TE, OFS)
6	Fine focus offset adjustment	CN204 (TP201), Pin1 (RF)	VR105 (FE, OFS)
7	Fine skew adjustment	CN204 (TP201), Pin1 (RF)	Radial tilt adjustment screw and Tangential tilt adjustment screw
8	Grating re-adjustment	CN104 (TP1), Pin3 (TE)	Grating adjustment slit

Adjustment 2

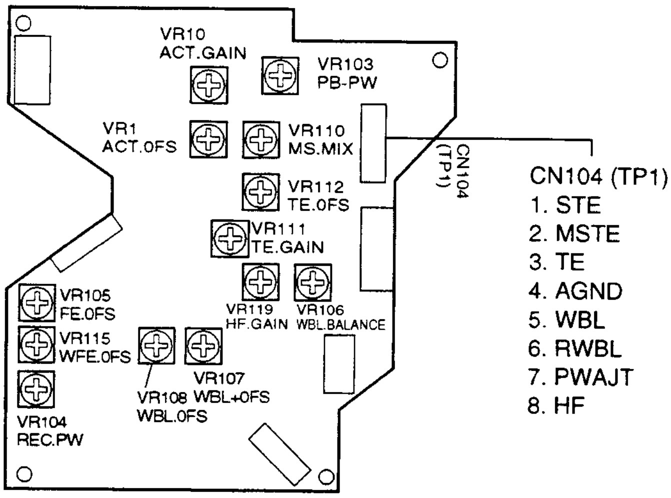
Step	Item	Test Point	Adjustment Location
1	WBL+offset adjustment	CN104 (TP1), Pin 6 (RWBL)	VR107 (WBL+. OFS)
2	Coarse WBL offset adjustment	CN104 (TP1), Pin 5 (WBL)	VR108 (WBL. OFS)
3	Playback power re-adjustment	CN104 (TP1), Pin 7 (PWAJT)	VR103 (PB. PW)
4	Coarse focus offset adjustment	CN204 (TP201), Pin 1 (RF)	VR105 (FE. OFS)
5	Main and sub mix ratio adjustment	CN104 (TP1), Pin 1 (STE) CN104 (TP1), Pin 2 (MSTE)	VR110 (MS. MIX)
6	Tracking amp. gain adjustment	CN104 (TP1), Pin 3 (TE)	VR111 (TE. GAIN)
7	Tracking offset adjustment	CN104 (TP1), Pin 3 (TE)	VR112 (TE. OFS)
8	ACT offset adjustment	CN5021 (TP00), Pin 1 (ACT ERR)	VR1 (ACT. OFS)
9	ACT GAIN adjustment	CN5021 (TP00), Pin 1 (ACT ERR)	VR10 (ACT. GAIN)
10	Fine focus offset adjustment	CN204 (TP201), Pin 1 (RF)	VR105 (FE. OFS)
11	WBL BALANCE adjustment	CN104 (TP1), Pin 5 (WBL)	VR106 (WBL. BALANCE)
12	Fine WBL offset adjustment	CN104 (TP1), Pin 5 (WBL)	VR108 (WBL. OFS)
13	WBL focus offset adjustment	CN104 (TP1), Pin 5 (WBL)	VR115 (WFE. OFS)
14	Recording power adjustment	CN104 (TP1), Pin 7 (PWAJT)	VR104 (REC. PW)
15	HF Amp. gain adjustment	CN104 (TP1), Pin 8 (HF)	VR119 (HF. GAIN)
16	Focus servo loop gain adjustment	CN204 (TP201), Pin 5 (FCSIN) CN204 (TP201), Pin 6 (FCSER)	VR201 (FCS. GAIN)
17	Tracking servo loop gain adjustment	CN204 (TP201), Pin 2 (TRKER) CN204 (TP201), Pin 3 (TRKIN)	VR202 (TE. GAIN)


1
3
CN5021
(TP00)
VR202
TE.GAIN
VR201
FCS.GAIN
TEST
MDOE
Short Land
6
1
CN204
(TP201)

CN5021 (TP00)
1. ACT ERR
2. ACT IN
3. V + 5A

CN204 (TP201)
1. RF
2. TRKER
3. TRKIN
4. A GND
5. FCSIN
6. FCSER

Fig. 1 SERVO UCOM BOARD ASSY


VR10
ACT.GAIN
VR103
PB-PW
VR1
ACT.OFS
VR110
MS.MIX
CN104
(TP1)
VR112
TE.OFS
VR111
TE.GAIN
VR105
FE.OFS
VR119
HF.GAIN
VR106
WBL.BALANCE
VR115
WFE.OFS
VR107
VR108 WBL+OFS
WBL.OFS
VR104
REC.PW

CN104 (TP1)
1. STE
2. MSTE
3. TE
4. AGND
5. WBL
6. RWBL
7. PWAJT
8. HF

Fig. 2 HEAD BOARD ASSY

● Notes

1. Use a 10:1 probe for the oscilloscope.
2. All the knob positions (settings) for the oscilloscope in the adjustment procedures are for when a 10:1 probe is used.

● Test Mode

This model has a test mode so that the adjustments and checks required for service can be carried out easily.
When this model is in test mode, the keys on the front panel work differently from normal. Adjustments and checks can be carried out by operating these keys with the correct procedure. For this model, all adjustments are carried out in test mode.

[Setting to Test Mode]

How to set this model into test mode.

1. Unplug the power cord from the AC socket.
2. Short the test mode short land. (See Fig. 1.)
3. Plug the power cord back into the AC socket.

When the test mode is set correctly, the display is different from what it usually is when the power is turned on. (lights up all FL display) If the display is still the same as usual, test mode has not been set correctly, so repeat Steps 1 – 3.

[Release from Test Mode]

Here is the procedure for releasing the test mode:

1. Press the STOP key and stop all operations.
2. Unplug the power cord from the AC socket.

[Operations of the keys in test mode]

Code	Key Name	Function In Test Mode	Explanation
	DIGITAL SYNCHRO	Playback laser diode ON	Lights up the laser diode by playback power.
	FINALIZE	Focus servo closes	The laser diode is lit up and the focus actuator is lowered, then raised slowly and the focus servo is closed at the point where the objective lens is focused on the disc. With the player in this state, if you lightly rotate the stopped disc by hand, you can hear the sound the focus servo. If you can hear this sound, the focus servo is operating correctly. If you press this key with no disc mounted, the laser diode lights up, the focus actuator is pulled down, then the actuator is raised and lowered three times and returned to its original position.

Code	Key Name	Function in Test Mode	Explanation
►	PLAY	Spindle servo ON	Starts the spindle motor in the clockwise direction and when the disc rotation reaches the prescribed speed (about 500 rpm at the inner periphery), sets the spindle servo in a closed loop.
❚❚	PAUSE	Tracking servo close/open	Pressing this key when the focus servo and spindle servo are operating correctly in closed loops puts the tracking servo into a closed loop, displays the track number being played back and the elapsed time on the front panel. If the elapsed time is not displayed or not counted correctly, it may be that something is out of adjustment, or that there is some other problem. This key is a toggle key and open/close the tracking servo alternately. This key has no effect if no disc is mounted.
◄◄ • |◄◄	MANUAL/ TRACK SEARCH REV	Carriage reverse (inwards)	Moves the pickup position toward the inner diameter of the disc. When this key is pressed with the tracking servo in a closed loop, the tracking servo automatically goes into an open loop. Since the motor does not automatically stop at the mechanical end point in test mode, be careful with this operation.
►► • ►►|	MANUAL/ TRACK SEARCH FWD	Carriage forward (outwards)	Moves the pickup position toward the outer diameter of the disc. When this key is pressed with the tracking servo in a closed loop, the tracking servo automatically goes into an open loop. Since the motor does not automatically stop at the mechanical end point in test mode, be careful with this operation.
■	STOP	Stop	Initializes and the disc rotation stops. The pickup and disc remain where they are when this key is pressed.
⏏	OPEN/CLOSE	Disc tray open/close	Open/close the disc tray. This key is a toggle key and open/close tray alternately. Pressing this key when the disc is turning stops the disc, then opens the tray. This key operation does not affect the position of the pickup.
○ ↓ ●	REC ↓ REC MUTE	Maximum recording power. Laser diode ON.	Lights up the laser diode with maximum recording power and normal EFM by pressing REC and REC MUTE keys in order. * The laser diode may be damaged if adjustments are made before pressing these keys.
	DISPLAY OFF	Focus offset switching	Switches the focus offset state. DISPLAY OFF LED LIGHTS UP : C/N in the best condition. LIGHTS OFF: Jitter in the best condition.
	WRITE	Optical axis servo switching	Switches the ON/OFF of the optical axis servo. (MANUAL) LED LIGHTS UP : Optical axis servo ON LIGHTS OFF: Optical axis servo OFF

[How to play back a disc in test mode]

In test mode, since the servos operate independently, playing back a disc requires that you operate the keys in the correct order to close the servos.
Here is the key operation sequence for playing back a disc in test mode.

FINALIZE	Lights up the laser diode and closes the focus servo.
⇩	
PLAY ▶	Starts the spindle motor and closes the spindle servo.
⇩	
PAUSE ❚❚	Closes the tracking servo.

Wait at least 2-3 seconds between each of these operations.

Adjustment 1

1. Playback Power Adjustment

Adjustment 1

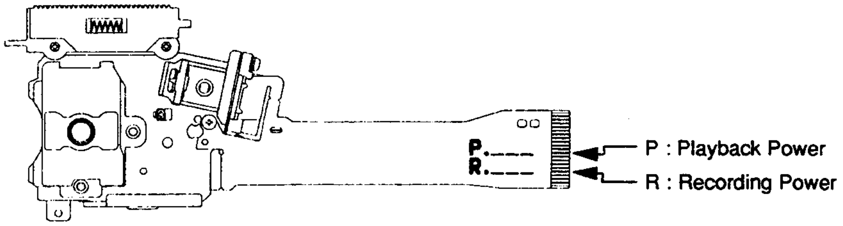
● Objective	To optimize the playback power of the laser diode.		
● Symptom when out of adjustment	Play does not start, track search is impossible, track are skipped.		
● Measurement instrument connections	Connect the multimeter to CN104 (TP1), Pin 7 (PWAJT)	● Player state	Test mode, Playback laser diode ON
		● Adjustment location	VR103 (PB. PW) (Head board assy)
		● Disc	None needed

[Procedure]

When adjusting with the multimeter
1. Light up the playback laser diode using the DIGITAL SYNCHRO key.
2. Adjust the voltage value of Pin 7 (PWAJT) of CN104 (TP1) to the voltage value (PB PW voltage ±5 mV) displayed on the pickup flexible cable using VR103 (PB PW).

Note) This adjustment cannot be performed accurately if disc is set. Be sure to remove disc first before adjustments.

Reference: When adjusting with the optical power meter
1. Move the pickup to the outer edge of the disc with the MANUAL/TRACK SEARCH FWD ►► ►►| key.
2. Lights up the playback laser diode by DIGITAL SYNCHRO key.
3. Shine the light discharged from the objective lens in the pickup on the light power meter sensor. Adjust VR103 (PB.PW) so that the playback laser diode output is an average 0.6 mW ± 0.05 mW.
   (Wavelength 790nm, Average mode)



* Recording on the disc is not possible in test mode.

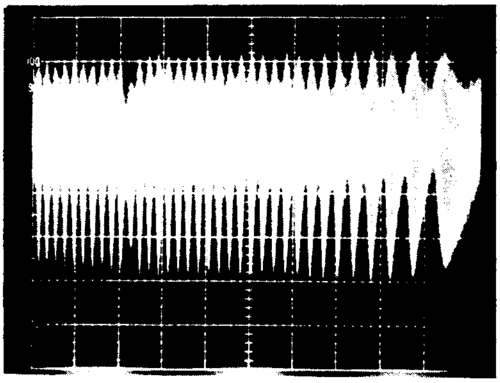
2. Coarse Focus Offset Adjustment

Adjustment 1

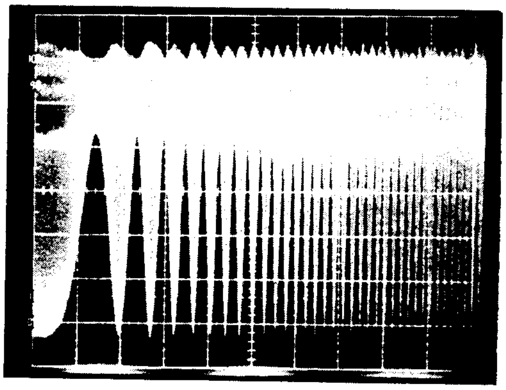
● Objective	To coarse adjust the DC offset voltage of the focus servo circuit for perform the tracking and slider adjustments correctly.		
● Symptom when out of adjustment	The model does not focus in, sound broken and the RF signal is dirty.		
● Measurement instrument connections	Connect the oscilloscope to CN204 (TP201), Pin 1 (RF) (SERVO UCOM board assy) [Settings] 20 mV/devision 2 ms/division DC mode	● Player state ● Adjustment location ● Disc	Test mode, focus and spindle servos closed and tracking servo open. VR105 (FE. OFS) (Head board assy) STD-903

[Procedure]

1. Press the FINALIZE key, then the PLAY ► key in that order to close the focus servo then the spindle servo.
2. Adjust VR105 (FE. OFS) so that the amplitude of waveform at CN204 (TP201), Pin 1 (RF) is maximum.



OUT of adjustment



Optimum adjustment

3. Coarse Skew Adjustment

Adjustment 1

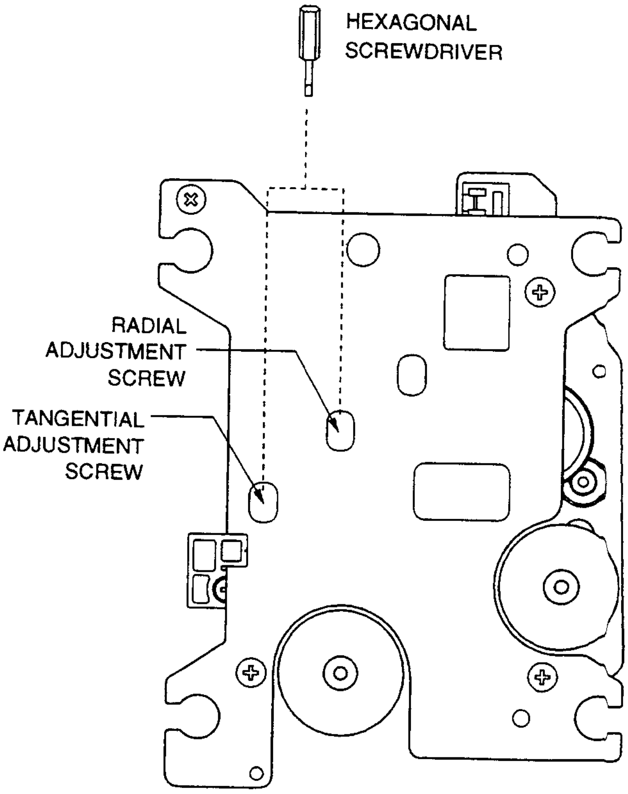
● Objective	To coarse adjust the angle of pickup to the disc for perform the grating and DPP (tracking offset) adjustments correctly.
● Symptom when out of adjustment	Sound broken, some discs can be played but not others.

● Measurement instrument connections	Connect the oscilloscope to CN204 (TP201), Pin 1 (RF). (SERVO UCOM board assy) [Settings] 20 mV/division 200 ns/division AC mode	● Player state	Test mode, focus and spindle servos closed and tracking servo open.
		● Adjustment location	Radial adjustment screw and tangential adjustment screw
		● Disc	STD-903

[Procedure]

1. Move the pickup to the position where the radial/ tangential adjustment screws will be seen with the MANUAL/TRACK SEARCH FWD ▶▶ ▶▶| or REV |◀◀ ◀◀ keys so that the radial/tangential adjustment screws can be adjusted.
2. Press the FINALIZE key, then the PLAY ▶ key in that order to close the focus servo then the spindle servo.
3. Adjust the RAD (radial direction) and TAN (tangential direction) adjustment screws alternately with hexagonal screwdriver (1.27 mm diagonal) to maximize the RF output at CN204 (TP201), pin 1.

Note: Radial direction and tangential direction mean the direction relative to the disc shown in Fig. 3.



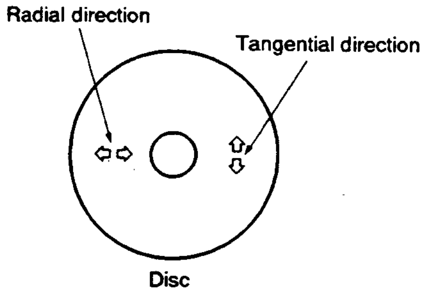


Fig. 3

4. Coarse Grating Adjustment

Adjustment 1

● Objective	To align the tracking error generation laser beam spots to the optimum angle on the track.		
● Symptom when out of adjustment	Play does not start, track search is impossible, tracks are skipped.		
● Measurement instrument connections	Connect the oscilloscope to CN104 (TP1), Pin 3 (TE) This connection may be via a low pass filter. (See Fig. 4) [Settings] 50 mV/division 5 ms/division DC mode	● Player state ● Adjustment location ● Disc	Test mode, focus and spindle servos closed and tracking servo open Grating slit on pickup STD-903

[Procedure]

1. Move the pickup to the position where the grating adjustment slit will be seen with the MANUAL/TRACK SEARCH FWD ▶▶ ▶▶| or REV |◀◀ ◀◀ keys so that the grating adjustment can be adjusted.
2. Press the FINALIZE key, then the PLAY ▶ key in that order to close the focus servo then spindle servo.
3. Insert a screwdriver into the grating adjustment slit and adjust the grating to find the null point.
   For more details, see next page.
4. If you slowly turn the screwdriver clockwise from the null point, the amplitude of the wave gradually increases, then if you continue turning the screwdriver, the amplitude of the wave becomes smaller again. Turn the screw driver counterclockwise from the null point and set the grating to the first point where the wave amplitude reaches its maximum.
   Reference : Fig.5 shows the relation between the angle of the tracking beam with the track and the waveform.
5. Return the pickup to more or less midway across disc with the MANUAL/TRACK SEARCH REV |◀◀ ◀◀ key, press the PAUSE II key and check that the track number and elapsed time are displayed on the front panel. If they are not displayed at this time or the elapsed time changes irregularly, check the null point and adjust the grating again.

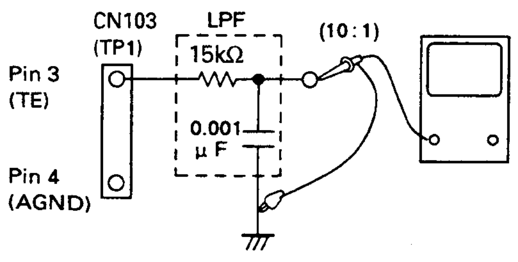
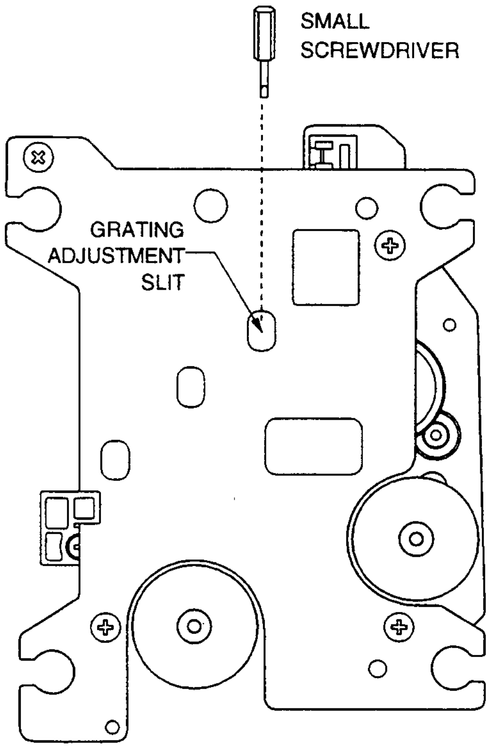


Fig. 4



[How to find the null point]

When you insert the small screwdriver into the slit for the grating adjustment and change the grating angle, the amplitude of the tracking error signal at CN104 (TP1), Pin 3 (TE) changes. Within the range for the grating, there are five or six locations where the amplitude of the wave reaches a minimum. Of these five or six locations, there is only one at which the envelope of the waveform is smooth. This location is where the three laser beams divided by the grating are all right above the same track. (See Fig. 5.)

This point is called the null point. When adjusting the grating, this null point is found and used as the reference position.

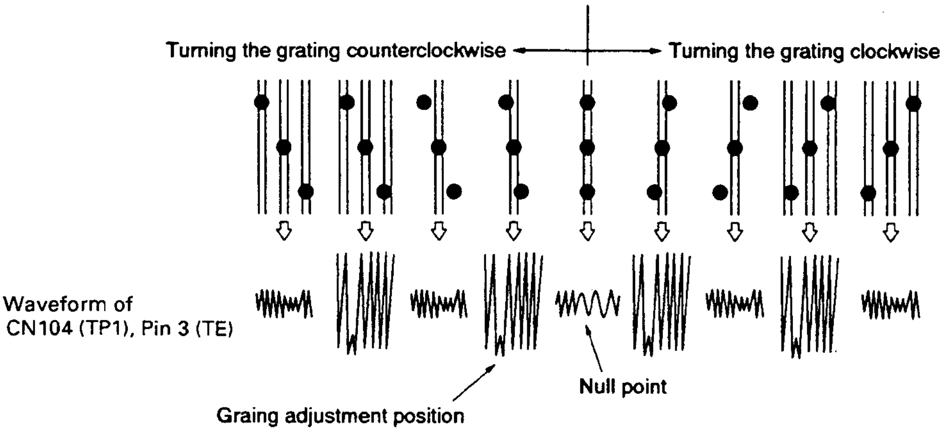
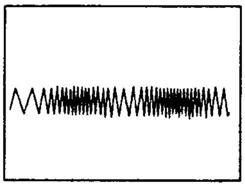
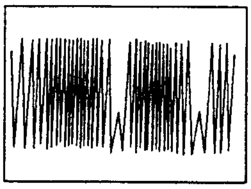

Turning the grating counterclockwise
Turning the grating clockwise
Waveform of CN104 (TP1), Pin 3 (TE)
Null point
Graing adjustment position

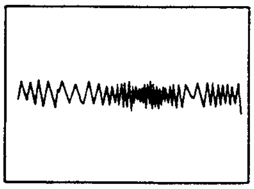
Fig. 5



Null point waveform



Maximum amplitude waveform



Waveform other than the null point

Note : If the difference between the amplitude of the error signal at the innermost edge and outermost edge of the disc is more than 10%, adjust the grating again.

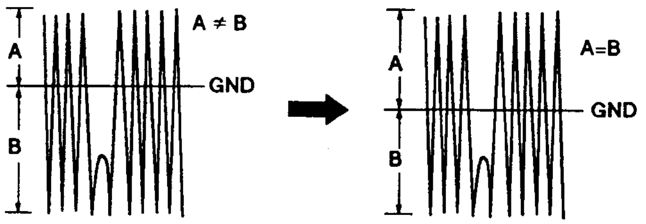
5. DPP (Tracking Offset) Adjustment

Adjustment 1

● Objective	To correct for the variation in the sensitivity of the tracking photodiode.		
● Symptom when out of adjustment	Player does not playback, track search is impossible, tracks are skipped.		
● Measurement instrument connections	Connect the oscilloscope to CN104 (TP1), Pin 3 (TE) [This connection may be via a low pass filter (15kΩ +0.001 μF).] [Settings] 50 mV/division 5 ms/division DC mode	● Player state	Test mode, focus and spindle servos closed and tracking servo open
		● Adjustment location	VR112 (TE. OFS) (Head board assy)
		● Disc	STD-903

[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ▶▶ ▶▶| or REV |◀◀ ◀◀ keys.
2. Press the FINALIZE key, then the PLAY ▶ key in that order to close the focus servo then the spindle servo.
3. Line up the bright line (ground) at the center of the oscilloscope screen and put the oscilloscope into DC mode.
4. Adjust VR112 (TE. OFS) so that the positive amplitude and negative amplitude of the tracking error signal at CN104 (TP1), Pin 3 (TE) are the same (in other words, so that there is no DC component).



When there is a DC component

When there is no DC component

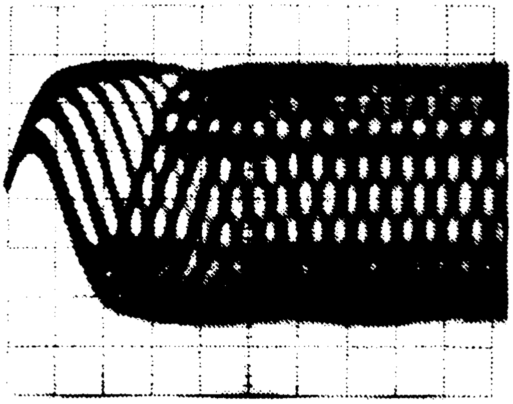
6. Fine Focus Offset Adjustment

Adjustment 1

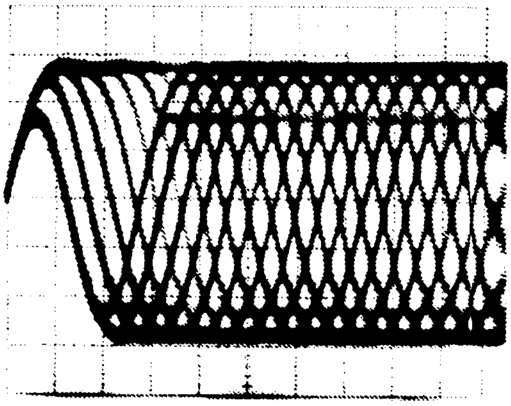
● Objective	To optimize the DC offset voltage of the focus servo circuit.		
● Symptom when out of adjustment	The player does not focus in, sound broken and the RF signal is dirty.		
● Measurement instrument connections	Connect the oscilloscope to CN204 (TP201), Pin 1 (RF). (SERVO UCOM board assy) [Settings] 20 mV/division 500 ns/division AC mode	● Player state	Test mode, play
		● Adjustment location	VR105 (FE. OFS) (Head board assy)
		● Disc	STD-903

[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ▶▶ ▶▶| or REV |◀◀ ◀◀ keys.
2. Press the FINALIZE key, the PLAY ▶ key, then the PAUSE ❚❚ key in that order to close the respective servos and put the player into play mode.
3. Adjust VR105 (FE. OFS) so that the 3T waveform at CN204 (TP201), Pin 1 (RF) is maximum.



Out of adjustment



Optimum adjustment

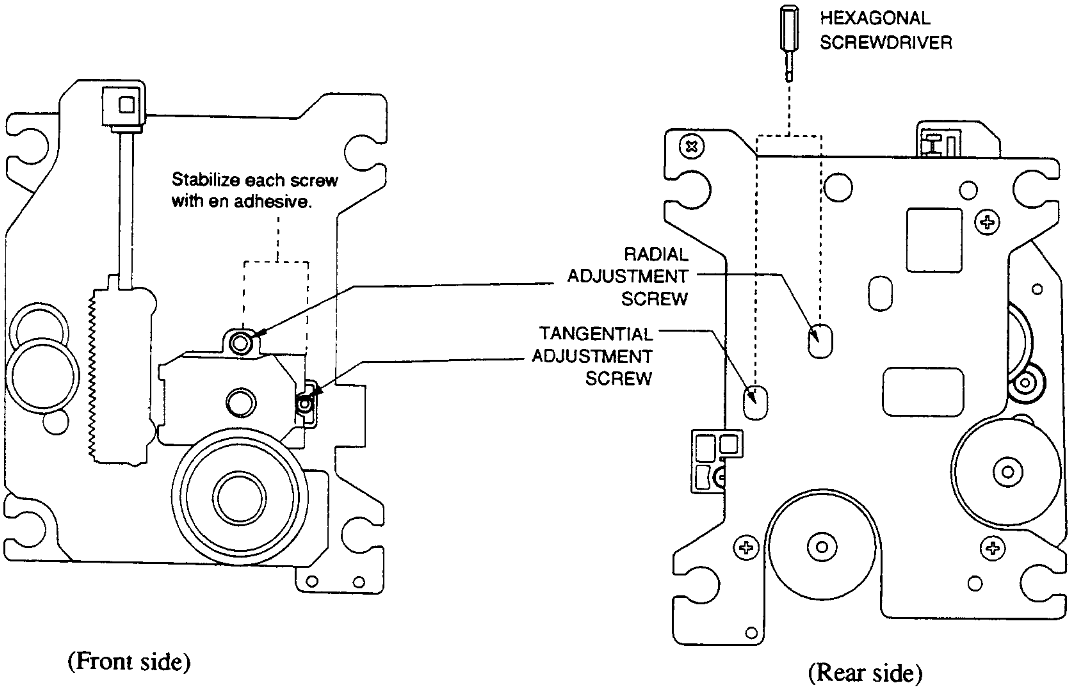
7. Fine Skew Adjustment

Adjustment 1

● Objective	To adjust the angle of the pickup relative to the disc so that the laser beams are shone straight down into the disc for the best read out of the RF signals.		
● Symptom when out of adjustment	Sound broken, some discs can be played but not others.		
● Measurement instrument connections	Connect the oscilloscope to CN204 (TP201), Pin 1 (RF). (SERVO UCOM board assy) [Settings] 20mV/division 200ns/division AC mode	● Player state ● Adjustment location ● Disc	Test mode, play Pickup radial adjustment screw and tangential adjustment screw STD-903

[Procedure]

1. Move the pickup to the position where the radial/tangential adjustment screws will be seen with the MANUAL/TRACK SEARCH FWD ►► ►►I or REV I◄◄ ◄◄ keys so that the radial/ tangential adjustment screws can be adjusted.
2. Press the FINALIZE key, then the PLAY ► key to the PAUSE II key in that order to close the respective servos and put the player into play mode.
3. First, adjust the radial adjustment screw with the hexagonal screwdriver (1.27 mm) so that the eye pattern (the diamond shape at the center of the RF signal) can be seen the most clearly.
4. Next, adjust the tangential adjustment screw with the hexagonal screwdriver so that the eye pattern can be seen the most clearly (Fig. 6).
5. Adjust in the order of the radial adjustment screw and the tangential screw again, so that the eye pattern can be seen the most clearly. As necessary, adjust the two screws alternately so that the eye pattern can be seen the most clearly.
6. After the adjustment, remove the float screw, turn over the servo mechanism assembly, then stabilize the radial adjustment screw and the tangential adjustment screw with an adhesive.


HEXAGONAL SCREWDRIVER
Stabilize each screw with en adhesive.
RADIAL ADJUSTMENT SCREW
TANGENTIAL ADJUSTMENT SCREW

(Front side)

(Rear side)

Adjustment 1

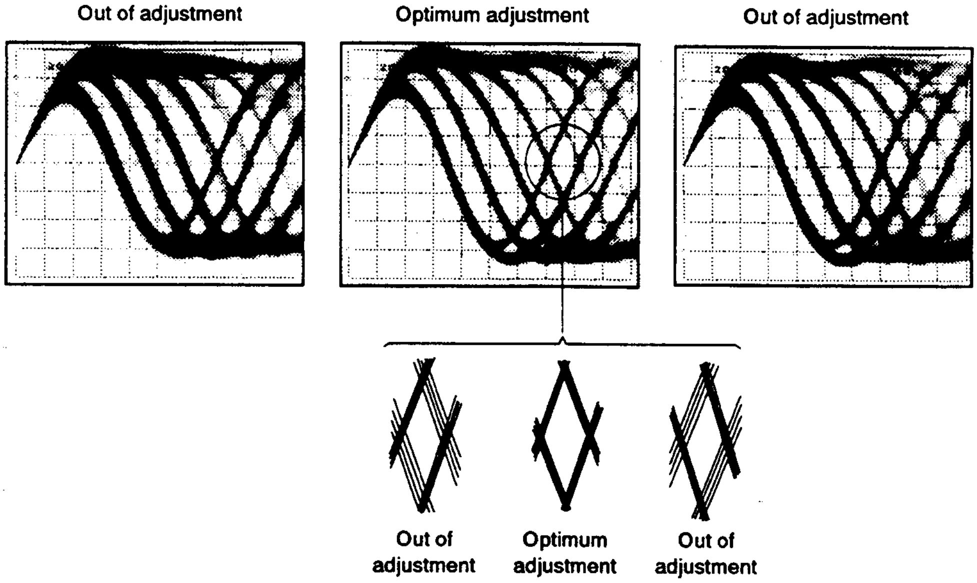

Out of adjustment
Optimum adjustment
Out of adjustment
Out of adjustment
Optimum adjustment
Out of adjustment

Fig.6 Eye pattern

8. Grating Re-Adjustment

Adjustment 1

Adjust in the same manner as "4. Coarse Grating Adjustment" in Adjustment 1.

Adjustment 2

1. WBL+Offset Adjustment

Adjustment 2

● Objective	To adjust the gain balance of the wobble signal.		
● Symptom when out of adjustment	Player does not record or playback CD-R discs.		
● Measurement instrument connections	Connect the oscilloscope to CN104 (TP1), Pin 6 (RWBL). (Head board assy) [Settings] 1 mV/division 5 ms/division DC mode	● Player state	Test mode, stop
		● Adjustment location	VR107 (WBL +. OFS) (Head board assy)
		● Disc	None needed

[Procedure]

1. Turn VR108 (WBL. OFS) to fully counterclockwise.
2. Adjust VR107 (WBL+. OFS) so that the DC voltage at CN104 (TP1), Pin 6 (RWBL) is –20mV±10mV.

2. Coarse WBL Offset Adjustment

Adjustment 2

● Objective	To optimize the DC offset voltage of the wobble amp.		
● Symptom when out of adjustment	Player does not record or playback CD-R discs.		
● Measurement instrument connections	Connect the oscilloscope to CN104 (TP1), Pin 5 (WBL). [Settings] 1 mV/division 5 ms/division DC mode	● Player state	Test mode, stop
		● Adjustment location	VR108 (WBL. OFS) (Head board assy)
		● Disc	None needed

[Procedure]

1. Adjust VR108 (WBL. OFS) so that the DC voltage at CN104 (TP1), Pin 5 (WBL) is 0±10mV.

3. Playback power Re-Adjustment

Adjustment 2

Adjust in the same manner as "1. Playback power Adjustment" in Adjustment 1.

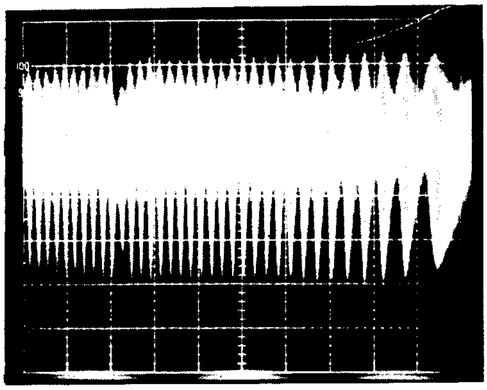
4. Coarse Focus Offset Adjustment

Adjustment 2

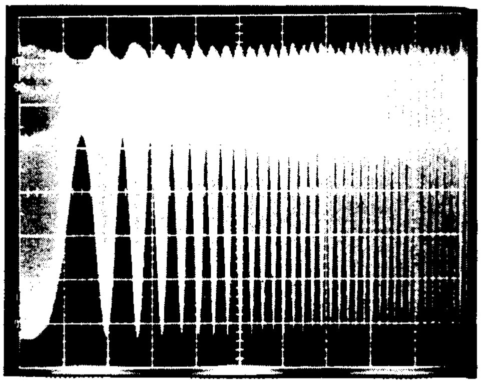
● Objective	To optimize the DC offset voltage of the focus error amp.		
● Symptom when out of adjustment	The player does not focus in and the RF signal is dirty.		
● Measurement instrument connections	Connect the oscilloscope to CN204 (TP201), Pin 1 (RF). (SERVO UCOM board assy)	● Player state	Test mode, focus and spindle servos closed and tracking servo open.
	[Settings] 20 mV/division 2m sec/division DC mode	● Adjustment location	VR105 (FE. OFS) (Head board assy)
		● Disc	STD-903

[Procedure]

1. Press the FINALIZE key, then the PLAY ► key in that order to close the focus servo then the spindle servo.
2. Adjust VR105 (FE. OFS) so that the amplitude of RF signal at CN204 (TP201), Pin 1 (RF) is maximum.



Out of adjustment



Optimum adjustment

5. Main and Sub Mix Ratio Adjustment

Adjustment 2

● Objective	To mix the gain of the main signal output and sub signal output of the pickup.		
● Symptom when out of adjustment	Player does not playback.		
● Measurement instrument connections	Connect the oscilloscope to CH1 : CN104 (TP1), Pin 1 (STE) CH2 : CN104 (TP1), Pin 2 (MSTE). [These connections must be via low pass filters.] [Settings] CH 1 : 50 mV/div. AC mode 10 ms/div. ADD mode CH 2 : 100 mV/div. AC mode	● Player state ● Adjustment location ● Disc	Test mode, focus and spindle servos closed and tracking servo open VR110 (MS. MIX) (Head board assy) STD-903

[Procedure]

1. Press the FINALIZE key, then the PLAY ▶ key in that order to close the focus servo then the spindle servo.
2. Set the oscilloscope to ADD mode (waveform adding mode of CH1 and CH2) and observe the adding waveform of CH1 and CH2.
3. Adjust VR110 (MS. MIX) so that the amplitude of waveform becomes minimum.

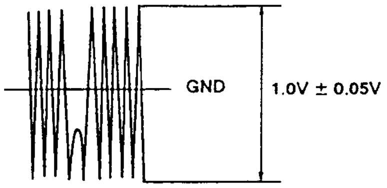
6. Tracking Amp. Gain Adjustment

Adjustment 2

● Objective	To correct the discrepancy in the tracking error level with the pickup.		
● Symptom when out of adjustment	Player does not playback, track search is impossible, tracks are skipped.		
● Measurement instrument connections	Connect the oscilloscope to CN104 (TP1), Pin 3 (TE). [This connection must be via a low pass filter (15kΩ+0.001μF).] [Settings] 20 mV/division 5 ms/division DC mode	● Player state ● Adjustment location ● Disc	Test mode, focus and spindle servos closed and tracking servo open VR111 (TE. GAIN) (Head board assy) STD-903

[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ▶▶ ▶▶| or REV |◀◀ ◀◀ keys.
2. Press the FINALIZE key, then the PLAY ▶ key in that order to close the focus servo then the spindle servo.
3. Line up the bright line (ground) at the center of the oscilloscope screen and put the oscilloscope into DC mode.
4. Adjust VR111 (TE. GAIN) so that the positive amplitude and negative amplitude of the tracking error signal at CN104 (TP1), Pin 3 (TE) is 1.0V±0.05V.



7. Tracking Offset Adjustment

Adjustment 2

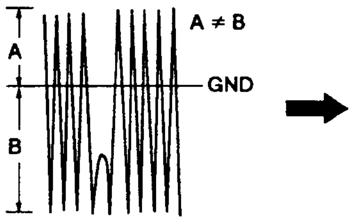
● Objective	To correct for the variation in the sensitivity of the tracking photodiode.
● Symptom when out of adjustment	Player does not playback, track search is impossible, tracks are skipped.

● Measurement instrument connections	Connect the oscilloscope to CN104 (TP1), Pin 3 (TE) [This connection must be via a low pass filter (15kΩ+0.001µF).] [Settings] 20 mV/division 5 ms/division DC mode	● Player state	Test mode, focus and spindle servos closed and tracking servo open
		● Adjustment location	VR112 (TE. OFS) (Head board assy)
		● Disc	STD-903

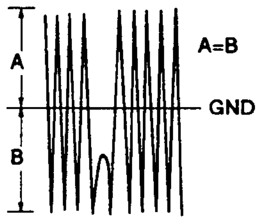
[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ►► ►►| or REV |◄◄ ◄◄ keys.
2. Press the FINALIZE key, then the PLAY ► key in that order to close the focus servo then the spindle servo.
3. Line up the bright line (ground) at the center of the oscilloscope screen and put the oscilloscope into DC mode.
4. Adjust VR112 (TE. OFS) so that the positive amplitude and negative amplitude of the tracking error signal at CN104 (TP1), Pin 3 (TE) are the same (in other words, so that there is no DC component).

Note : Perform the run-on adjustment in the section 6 and 7.



When there is a DC component



When there is no DC component

8. ACT offset Adjustment

Adjustment 2

● Objective	To optimize the DC offset voltage of the actuater servo.		
● Symptom when out of adjustment	Player does not pause, track search is impossible, tracks are skipped.		
● Measurement instrument connections	Connect the oscilloscope to CN5021 (TP00), Pin 1 (ACT ERR) (SERVO UCOM board assy) [Settings] 5mV/division 5 ms/division DC mode	● Player state	Test mode, focus and spindle servos closed and tracking servo open
		● Adjustment location	VR1 (ACT. OFS) (Head board assy)
		● Disc	STD-903

[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ►► ►►| or REV |◄◄ ◄◄ keys.
2. Press the FINALIZE key, then the PLAY ► key in that order to close the focus servo then the spindle servo.
3. Adjust VR1 (ACT. OFS) so that the DC voltage at CN5021 (TP00), pin 1 (ACT ERR) is 0±20mV.

9. ACT GAIN Adjustment

Adjustment 2

● Objective	To optimize the actuater servo gain.		
● Symptom when out of adjustment	Player does not pause, track search is impossible, tracks are skipped.		
● Measurement instrument connections	Connect the oscilloscope to CN5021 (TP00), Pin 1 (ACT ERR) (SERVO UCOM board assy) [Settings] 10mV/division 5 ms/division DC mode	● Player state	Test mode, focus and spindle servos closed and tracking servo open
		● Adjustment location	VR10 (ACT. GAIN) (Head board assy)
		● Disc	STD-903

[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ►► ►►| or REV |◄◄ ◄◄ keys.
2. Press the FINALIZE key, then the PLAY ► key in that order to close the focus servo then the spindle servo.
3. Press the WRITE key to light up the WRITE KEY LED, and short-circuit the Pin 2 and Pin 3 of CN5021 (TP00).
4. Adjust VR10 (ACT. GAIN) so that the DC voltage at CN5021 (TP00), Pin 1 (ACT ERR) is −380±20mV.

Note: Perfom the run-on adjustment in the section 8 and 9.

10. Fine Focus Offset Adjustment

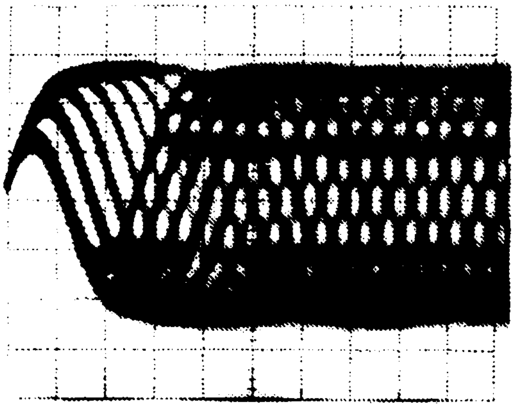
Adjustment 2

● Objective	To optimize the DC offset voltage of the focus servo circuit.		
● Symptom when out of adjustment	The player does not focus in, sound broken and the RF signal is dirty.		
● Measurement instrument connections	Connect the oscilloscope to CN204 (TP201), Pin 1 (RF). (SERVO UCOM board assy) [Settings] 20 mV/division 500 ns/division AC mode	● Player state	Test mode, play
		● Adjustment location	VR105 (FE. OFS) (Head board assy)
		● Disc	STD-R03

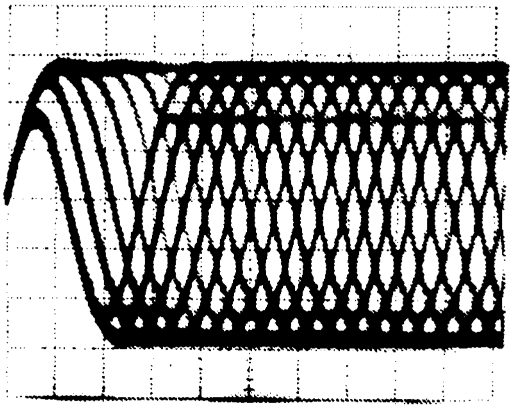
[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ►► ►►| or REV |◄◄ ◄◄ keys.
2. Press the FINALIZE key, the PLAY ► key, then the PAUSE II key in that order to close the respective servos and put the player into play mode.
3. Adjust VR105 (FE. OFS) so that the 3T waveform at CN204 (TP201), Pin 1 (RF) is maximum.

Note) Adjust after confirming that the WRITE KEY LED is OFF.



Out of adjustment



Optimum adjustment

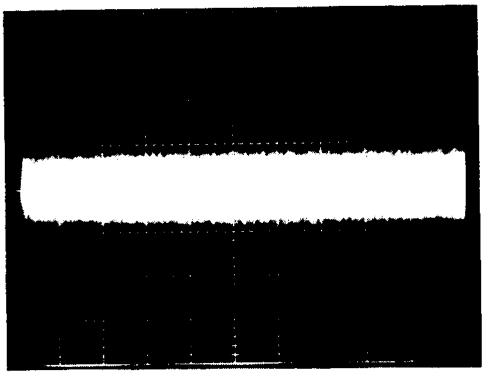
11. WBL BALANCE Adjustment

Adjustment 2

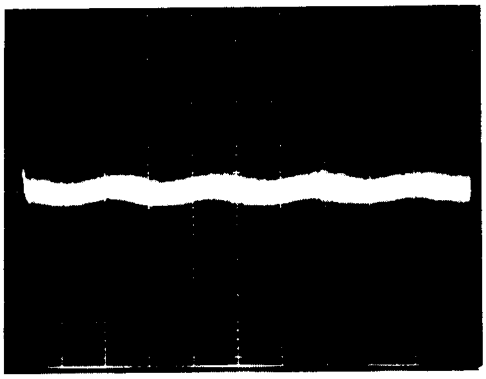
● Objective	To adjust the gain balance of the wobble signal.		
● Symptom when out of adjustment	Player does not record or search or pause CD-R discs.		
● Measurement instrument connections	Connect the oscilloscope to CN104 (TP1), Pin 5 (WBL). [This connection must be via a high-pass filter (180pF+3.9kΩ).]	● Player state	Test mode, play
		● Adjustment location	VR106 (WBL. BALANCE) (Head board assy)
	[Settings] 5mV/division 20µsec/division DC mode	● Disc	STD-R03

[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ►► ►►I or REV I◄◄ ◄◄ keys.
2. Press the FINALIZE key, the PLAY ► key, then the PAUSE II key in that order to close the respective servos and put the player into play mode.
3. Adjust VR106 (WBL. BALANCE) so that the amplitude of the waveform at CN104 (TP1), Pin 5 (WBL) is minimum.



Out of adjustment



Optimum adjustment

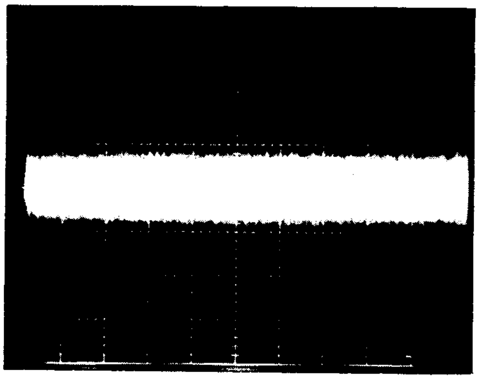
12. Fine WBL offset Adjustment

Adjustment 2

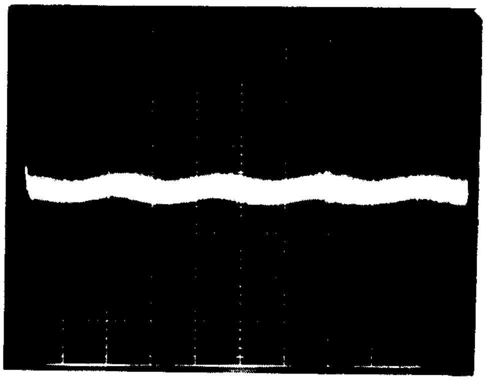
● Objective	To adjust the gain balance of the wobble signal.		
● Symptom when out of adjustment	Player does not record or search or pause CD-R discs.		
● Measurement instrument connections	Connect the oscilloscope to CN104 (TP1), Pin 5 (WBL) [This connection must be via a high-pass filter (180pF+3.9kΩ)] [Settings] 5mV/division 20μsec/division DC mode	● Player state	Test mode, play
		● Adjustment location	VR108 (WBL. OFS) (Head board assy)
		● Disc	STD-R03

[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ►► ►►| or REV |◄◄ ◄◄ keys.
2. Press the FINALIZE key, the PLAY ► key, then the PAUSE II key in that order to close the respective servos and put the player into play mode.
3. Adjust VR108 (WBL. OFS) so that the waveform at CN104 (TP1), Pin 5 (WBL) is minimum.



Out of adjustment



Optimum adjustment

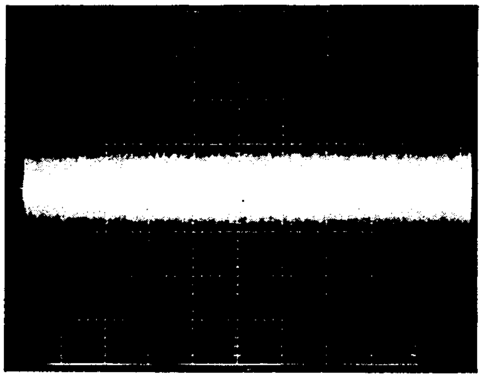
13. WBL focus offset Adjustment

Adjustment 2

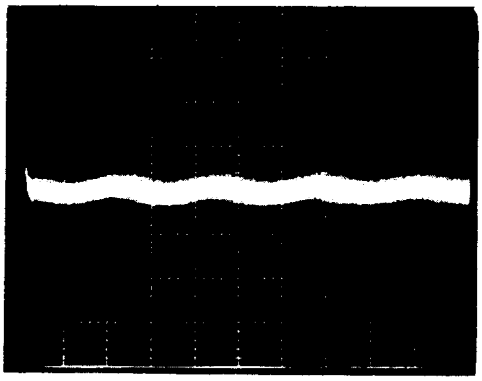
● Objective	To adjust the gains balance of the wobble signal.		
● Symptom when out of adjustment	Player does not record or search or pause CD-R discs.		
● Measurement instrument connections	Connect the oscilloscope to CN104 (TP1), Pin 5 (WBL). [This connection must be via a high-pass filter (180pF+3.9kΩ).] [Settings] 5mV/division 20µsec/division DC mode	● Player state	Test mode, play
		● Adjustment location	VR115 (WFE. OFS) (Head board assy)
		● Disc	STD-R03

[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ►► ►►| or REV |◄◄ ◄◄ keys.
2. Press the FINALIZE key, the PLAY ► key, then the PAUSE II key in that order to close the respective servos and put the player into play mode.
3. Press the DISPLAY OFF key to light up the DISPLAY OFF KEY LED.
4. Adjust VR115 (WFE. OFS) so that the amplitude of the waveform at CN104 (TP1), Pin 5 (WBL) is minimum.



Out of adjustment



Optimum adjustment

14. Recording Power Adjustment

Adjustment 2

● Objective	To optimize the recording power of the laser diode.
● Symptom when out of adjustment	The player does not record nor playback self-recorded discs. It also skips tracks and the RF waveform is dirty. (No problems during CD playback)

● Measurement instrument connections	Connect the multimeter to CN104 (TP1), Pin 7 (PWAJT).	● Player state	Test mode, maximum recording power ON
		● Adjustment location	VR104 (REC. PW) (Head board assy)
		● Disc	None needed

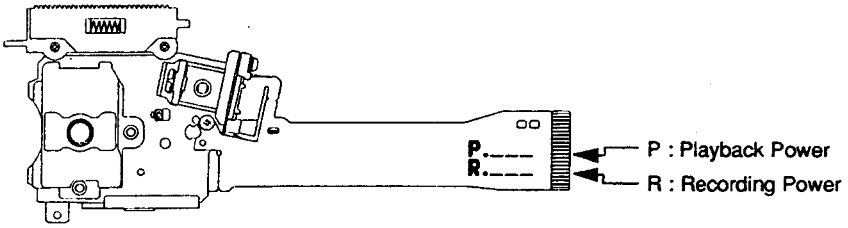
[Procedure]

When adjusting with the multimeter

1. Fully turn VR104 (REC. PW) counterclockwise to reduce the power to the minimum.
2. Press REC ○ and REC MUTE ○ keys in this order to lights up the laser diode.
3. Adjust the voltage value of Pin 7 (PWAJT) of CN104 (TP1) to the voltage value (REC. PW voltage ±10 mV) displayed on the pickup flexible cable using VR104 (REC. PW).

Notes

- Power more than ten times greater than playback power is released during these adjustment
  Never look directly at the objective lens.
- This adjustment cannot be performed accurately if disc is set. Be sure to remove disc first before adjustments.
- Perform this adjustment more than two minutes after starting up the test mode (after inserting the AC plug).
- The laser diode may be damaged if the recording power is greater than the specified value.
  Always perform step 1 before making adjustments and be careful not to exceed the adjustment value by more than 50mV (specified value in step 3).



Reference : When adjusting with optical power meter.

1. Fully turn VR104 (REC. PW) counterclockwise to reduce the power to the minimum.
2. Move the pickup to the outer edge of the disc with the MANUAL/TRACK SEARCH FWD ►► ►►| key.
3. Press REC ○ and REC MUTE ○ keys in that order to lights up the laser diode.
4. Shine the light discharged from the objective lens in the pickup on the light power meter sensor and adjust VR104 (REC. PW) so that the recording laser diode output is an average of 4.5mW±0.1mW (Wavelength 790nm, Average mode).

Notes

- Perform this adjustment more than two minutes after starting up the test mode (after inserting the AC plug)
- The laser diode may be damaged if the recording power is greater than the specified value.
  Always perform step 1 before making adjustments and be careful not to exceed the adjustment value by more than 0.3mW (specified value in step 3).
- Power more than ten times greater than playback power is released during these adjustment
  Never look directly at the objective lens.

15. HF Amp. Gain Adjustment

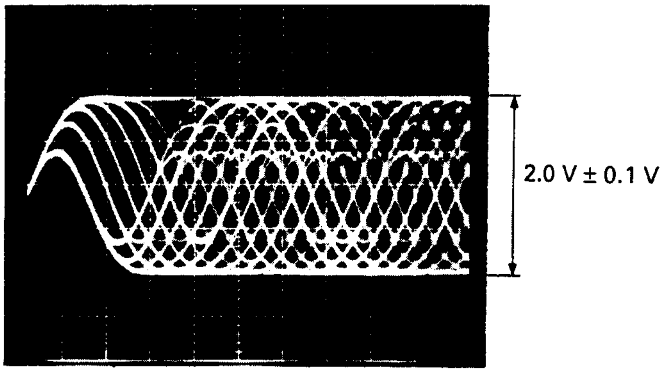
Adjustment 2

● Objective	To correct the discrepancy in the HF level with the pickup.		
● Symptom when out of adjustment	Player does not record, track search is impossible.		
● Measurement instrument connections	Connect the oscilloscope to CN104 (TP1), Pin 8 (HF).	● Player state	Test mode, play
		● Adjustment location	VR119 (HF. GAIN) (Head board assy)
	[Settings] 50 mV/division 500nsec/division DC mode	● Disc	STD-903

[Procedure]

1. Move the pickup to midway acrosss the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ▶▶ ▶▶| or REV |◀◀ ◀◀ keys.
2. Press the FINALIZE key, the PLAY ▶ key, then the PAUSE ❚❚ key in that order to close respective servos and put the player into PLAY mode.
3. Line up the bright line (ground) at the center of the oscilloscope screen and put the oscilloscope into DC mode.
4. Adjust VR119 (HF. GAIN) so that the amplitude of the waveform at CN104 (TP1), Pin 8 (HF) is 2.0V ± 0.1 V.

Note) Adjust after checking that the DISPLAY OFF KEY LED is OFF.



16. Focus Servo Loop Gain Adjustment

Adjustment 2

● Objective ● Symptom when out of adjustment	To optimize the focus servo loop gain. Playback does not start or focus actuator noisy.		
● Measurement instrument connections —	See Fig. 7 (SERVO UCOM board assy) [Settings] CH 1 : 0.1 V/division X-Y mode CH 2 :10 mV/division	● Player state ● Adjustment location ● Disc	Test mode, play VR201 (FCS. GAIN) (SERVO UCOM board assy) STD-903

[Procedure]

1. Set the AF generator output to 1.4kHz and 1Vp-p.
2. Move the pickup to midway across the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ▶▶ ▶▶| or REV |◀◀ ◀◀ keys.
3. Press the FINALIZE key, the PLAY ▶ key, then the PAUSE ❚❚ key in that order to close the respective servos and put the player into play mode.
4. Adjust VR201 (FCS. GAIN) so that the lissajous waveform is symmetrical about the X axis and the Y axis.

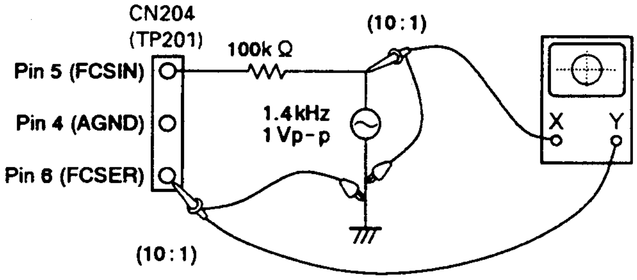
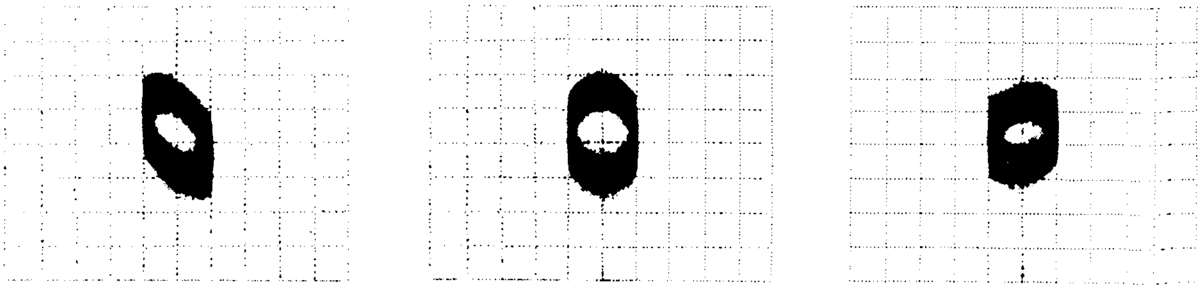


Fig. 7



Higher gain

Optimum gain

Lower gain

17. Tracking Servo Loop Gain Adjustment

Adjustment 2

● Objective	To optimize the tracking servo loop gain.		
● Symptom when out of adjustment	Playback does not start, during searches the actuator is noisy, or tracks are skipped.		
● Measurement instrument connections	See Fig. 8 (SERVO UCOM board assy) [Settings] CH 1 : 0.1 V/division X-Y mode CH 2 :10 mV/division	● Player state	Test mode, play
		● Adjustment location	VR202 (TE. GAIN) (SERVO UCOM board assy)
		● Disc	STD-903

[Procedure]

1. Set the AF generator output to 1.2kHz and 2Vp-p.
2. Move the pickup to midway across the disc (R=35mm) with the MANUAL/TRACK SEARCH FWD ▶▶ ▶▶| or REV |◀◀ ◀◀ keys.
3. Press the FINALIZE key, the PLAY ▶ key, then the PAUSE ❚❚ key in that order to close the respective servos and put the player into play mode.
4. Adjust VR202 (TE. GAIN) so that the lissajous waveform is symmetrical about the X axis and the Y axis.

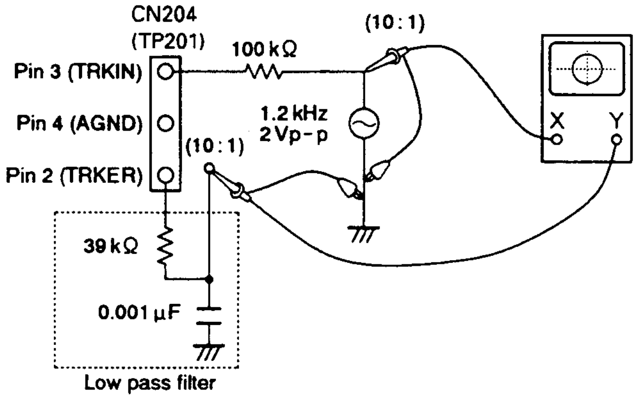
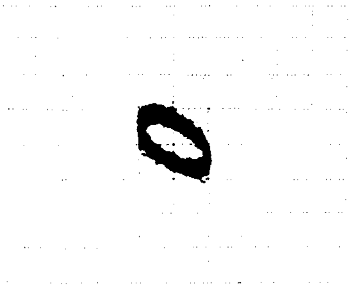
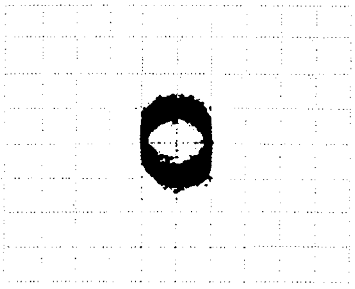

CN204
(TP201)
Pin 3 (TRKIN)
Pin 4 (AGND)
Pin 2 (TRKER)
100 kΩ
(10:1)
1.2 kHz
2Vp-p
(10:1)
X
Y
39 kΩ
0.001 μF
Low pass filter

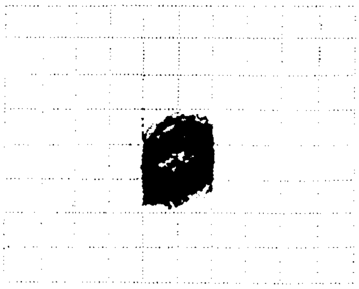
Fig. 8



Higher gain



Optimum gain



Lower gain

8. TROUBLESHOOTING

8.1 Service Number Display

This unit displays "CHECK" or "CHECK" "DISC?" during abnormal operations and stops.

When the STOP key or CLEAR key of the remote control unit is pressed continuously for about 10 seconds, the last service number will be displayed.

To correct the error, check the peripheral circuits mainly for the check point devices.

8.2 Service Codes and Countermeasures

Code	Contents	Location of Fault	Cause	Checkpoint
H0 H1	Unit does not operate even when the cord is inserted into outlet. (CHECK displayed)	H0: Communication is NG in mechanism controller, mode controller. H1: Mechanism controller detected fault in circuit.	• Faulty soldering • Pattern short-circuit • Parts short-circuit • Faulty power	IC356, IC357, IC207, IC358, IC352, IC353
H2	Recording preparations cannot be performed, tray does not open. (CHECK displayed)	H2: Mechanism controller pins 22, 23, 24 pin input voltage error		IC205
H5	Recording impossible (CHECK displayed)	IC360	• IC360 fault	IC360
L*	Unit stops during tray open/close. (CHECK displayed)	Loading section fault has been detected	• Faulty tray position sensor • Faulty loading motor • Faulty soldering, pattern short-circuit • Pattern short-circuit, faulty power	IC203
E*	Operations stop when disc is inserted, playback start is requested, REC/P is requested, and operations are acknowledged. (CHECK displayed)	Slider section fault has been detected • Pickup could not be moved to designated position.	• Flexible cable absent • Faulty drive circuit • Faulty TOC position SW • Faulty soldering, pattern short-circuit • Pattern short-circuit, faulty power	D1001, IC203, IC201, IC206
P*	Unit stops when disc is inserted without reading the internal information. (CHECK displayed)	Spindle section fault has been detected. • Back side of disc has been inserted. • Disc with scratches or dusts has been inserted. • Disc could not be rotated normally. • Designated signal could not be obtained from disc.	• Faulty spindle motor • Faulty spindle drive circuit • Error in FG detection • Faulty WBL circuit • Faulty decoder circuit • ATIP, sub codes cannot be read. • Error rate is high.	PC1001, IC202, IC201, IC206
C*	Operations stop before REC/P is set. (CHECK displayed)	Recording laser power related fault has been detected • Disc with scratches or dusts has been inserted. • Proper recording power is not output. • RF detection is not normal.	• Faulty laser diode. • Error in RF detection. • Faulty RFT, RFB circuit. • Insufficient recording power. • Faulty soldering, pattern short-circuit • Pattern short-circuit, faulty power • This error also occurs when ATIP, sub codes cannot be read.	IC205, IC101, IC362, IC363
F*	Operations stop during playback or recording. (CHECK displayed)	Pickup section fault has been detected. • Disc with scratches or dusts has been inserted and therefore no focus. • Proper laser power is not output. • No focus.	• Faulty laser diode. • Faulty focus drive circuit. • Faulty pickup. • Faulty soldering, pattern short-circuit • Pattern short-circuit, faulty power.	IC206, IC203

Code	Symptom	Location of Fault	Cause	Checkpoint
A*	CHECK DISC is displayed and unit stops during recording related operations.	Stop has been detected during recording. • Disc scratches, dusts, etc. are obstructing operations and unit has stopped.	If hardware problems have occurred, before A* and d* numbers are generated, codes other than those above are generated and the unit stops. Consequently, these service codes are generated only when operational problems have occurred due to the disc. Faulty soldering, pattern short-circuit Possible if pattern has short-circuit or power is faulty.	
d*	CHECK DISC is displayed and unit stops during recording related operations. Disc internal information cannot be read and unit stops when disc is inserted.	Stop has been detected during recording. • Disc scratches, dusts, etc. are obstructing operations and unit has stopped.		

Note) * indicates the mechanism mode and are the following numbers.

No.	Mechanism Mode	No.	Mechanism Mode	No.	Mechanism Mode
0	PLAY	5	Setup	A	REC
1	OPEN	6	TOC read	B	TOC REC
2	STOP	7	—	C	OPC
3	—	8	Search	D	TOC check
4	—	9	REC/PAUSE	E	PMA, actual pause recording

9. IC INFORMATION

• The information shown in the list is basic information and may not correspond exactly to that shown in schematic diagrams.

■ PD4584A (SERVO UCOM BOARD ASSY, IC356) Mechanism Control Microcomputer

● Pin Function

Pin No.	Mark	Name	I/O	Initial	Function
1	P43/AD3	AD3	I/O	—	Data address line
2	P44/AD4	AD4	I/O	—	
3	P45/AD5	AD5	I/O	—	
4	P46/AD6	AD6	I/O	—	
5	P47/AD7	AD7	I/O	—	
6	P50/A8	A8	O	—	Address line
7	P51/A9	A9	O	—	
8	P52/A10	A10	O	—	
9	P53/A11	A11	O	—	
10	P54/A12	A12	O	—	
11	P55/A13	A13	O	—	
12	NC	GND	—	—	Not used
13	P56/A14	A14	O	—	Address line
14	P57/A15	A15	O	—	
15	Vdd	+5V	—	—	Positive power supply voltage
16	AVss	GND	—	—	A/D converter GND
17	P70/AN0	XOPEN	I	—	OPEN SW. "L" when open is completed
18	P71/AN1	XCLMP	I	—	CLAMP SW. "L" when clamp DOWN
19	NC	GND	—	—	Not used
20	P72/AN2	GND	I	—	
21	P73/AN3	GND	I	—	
22	P74/AN4	TEPP	I (A)	—	Tracking error peak to peak (For trracking gain adjustment)
23	P75/AN5	RFT	I (A)	—	Playback RF upper envelope
24	P76/AN6	RFB	I (A)	—	Playback RF lower envelope
25	P77/AN7	MACK	I	—	"L" when opposite mode controller serial handshake is input
26	AVref	+5V	—	—	A/D converter reference voltage input
27	AVdd	+5V	—	—	A/D converter analog power supply
28	Vdd	+5V	—	—	Positive power supply pin
29	P20/NM1	XPFAIL	I	—	"L" when power failure is detected. ↓ detection
30	P21/INTP0	FG	I	—	Spindle FG ↓ detection
31	P22/INTP1	SCOR	I	—	EFM decoder frame sync ↓ detection
32	P23/INTP2	ATIP	I	—	ATIP sync ↑ ↓ detection
33	P24/INTP3	ESYN	I	—	EFM encoder frame sync ↓ detection
34	P25/INTP4	XRFDT	I	—	"L" when EFM playback RF detected. ↓ detection
35	P26/INTP5	TOCP	I	—	TOC position sensor (For slider stop processing at TOC position (=L))
36	P27/INTP3/TI	SENS	I	—	SONY servo IC SENS signal (For details, refer to 7. Timing Chart.)
37	NC	GND	—	—	Not used
38	P30/TxD	FOK	I	—	Focus OK input ("H" when Focus OK)
39	P31/RxD	XECE	O	H	"L" when test tool reading enable is output
40	P32/SO/SBO	MSO	O	L	Clock sync serial transformer data output)

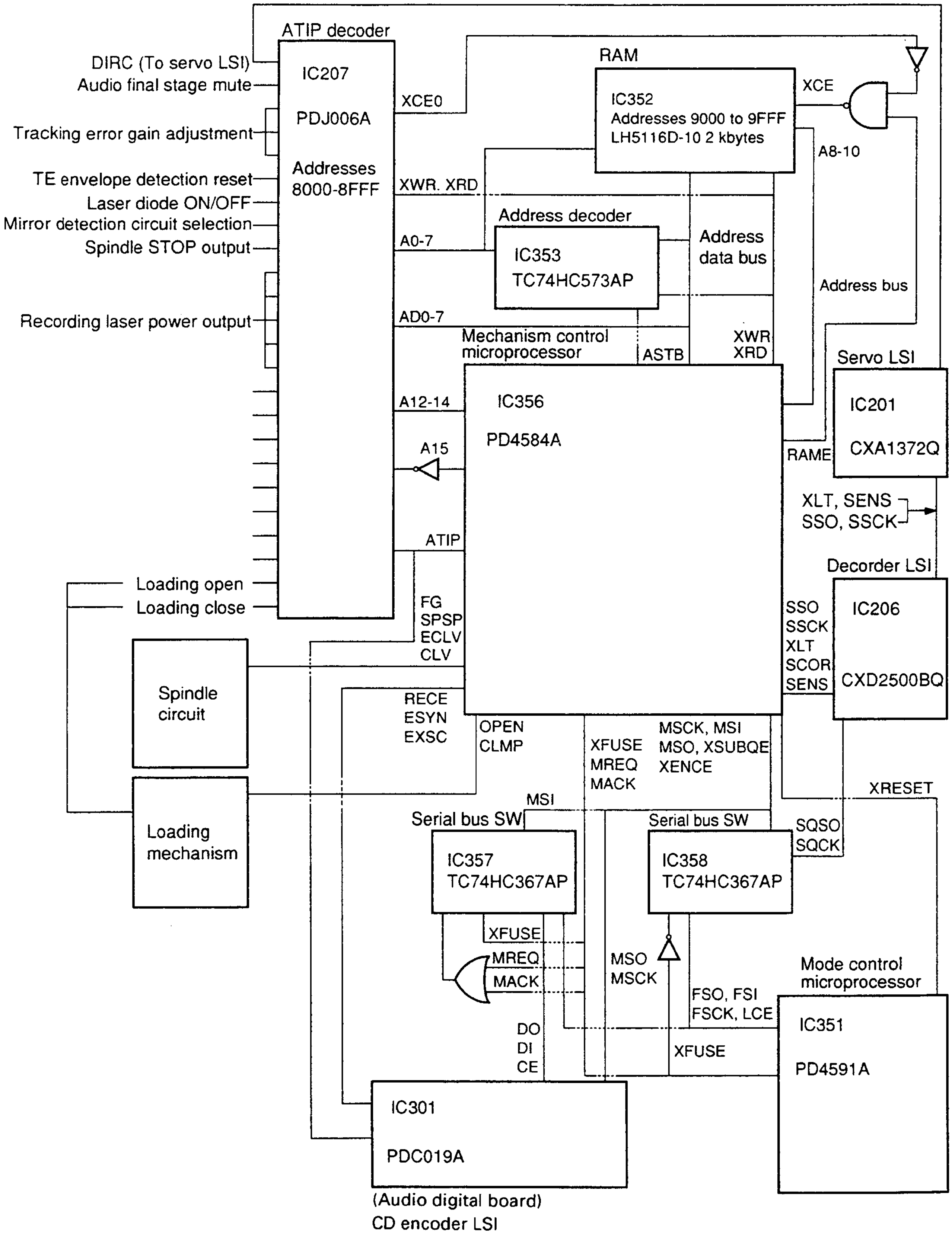
Note) "A" in the I/O column indicates analog.

Pin No.	Mark	Name	I/O	Initial	Function
41	P33/SI/SBI	MSI	I	L	Clock sync serial transfer data input
42	P34/$\overline{\text{SCK}}$	MSCK	O	H	Clock sync serial transfer clock output
43	NC	GND	—	—	Not used
44	P80/T000	XFUSE	I	H	"L" when communication between PDC019 ⇔ Mode contoroller
45	P81/T001	GFS	I	—	GFS input ("H" when GFS OK)
46	P82/T002	ECLV	O	H	Spindle servo EFM/Wobble CLV mode
47	P83/T003	CLV	O	H	Spindle servo CLV/CAV mode
48	P84/T010	SPSQ	O	—	Spindle drive PWM output during spindle CAV
49	P85/T001	MREQ	O	H	"L" when opposite mode controller serial handshake is output
50	$\overline{\text{RESET}}$	XRST	I	—	"L" when reset input
51	X1	CLOCK	I	—	System clock oscillation crystal connection pin Input to X1 pin when clock is supplied from outside
52	X2	CLOCK	—	—	
53	NC	GND	—	—	Not used
54	Vss	GND	—	—	GND pin
55	$\overline{\text{WDTO}}$	NC	O	L	Not used
56	P00/RTP0	XSUBQE	O	H	"L" when EFM decoder sub code Q reading is enabled
57	NC	GND	—	—	Not used
58	P01/RTP1	XENCE	O	L	"H" when PDC019 serial enable is output
59	P02/RTP2	XASYN	O	L	ATIP frame sync "L"
60	P03/RTP3	XEXSC	O	H	"L" when PDC019 external sync enable is output
61	P04/RTP4	SSO	O	L	SONY servo IC command special serial data output
62	P05/RTP5	SSCK	O	H	SONY servo IC command special serial clock output
63	P06/RTP6	XLT	O	H	"L" when SONY servo IC command is latched
64	P07/RTP7	RECE	O	L	"H" when laser diode recording power is on
65	$\overline{\text{EA}}$/Vpp	$\overline{\text{EA}}$	I	—	Used as internal ROM mode when connected to +5V
66	Vss	GND	—	—	GND pin
67	P93/TMD	RAME	O	H	"H" when external SRAM is enable
68	P92/$\overline{\text{TAS}}$	XSVRST	O	L	"L" when servo system IC mode control reset is output
69	P91/$\overline{\text{WR}}$	XWR	O	L	Strobe signal output for external memory write operations
70	P90/$\overline{\text{RD}}$	XRD	O	L	Strobe signal output for external memory read operations
71	ASTB	ASTB	O	—	Signal which latches lower address signal for external memory access externally
72	P40/ADD	AD0	I/O	—	Data address line
73	P41/AD1	AD1	I/O	—	
74	P42/AD2	AD2	I/O	—	

1. "External Port"-output from PDJ006A (SERVO UCOM BOARD ASSY, IC207) (External RAM area (8000H to 8FFFH)

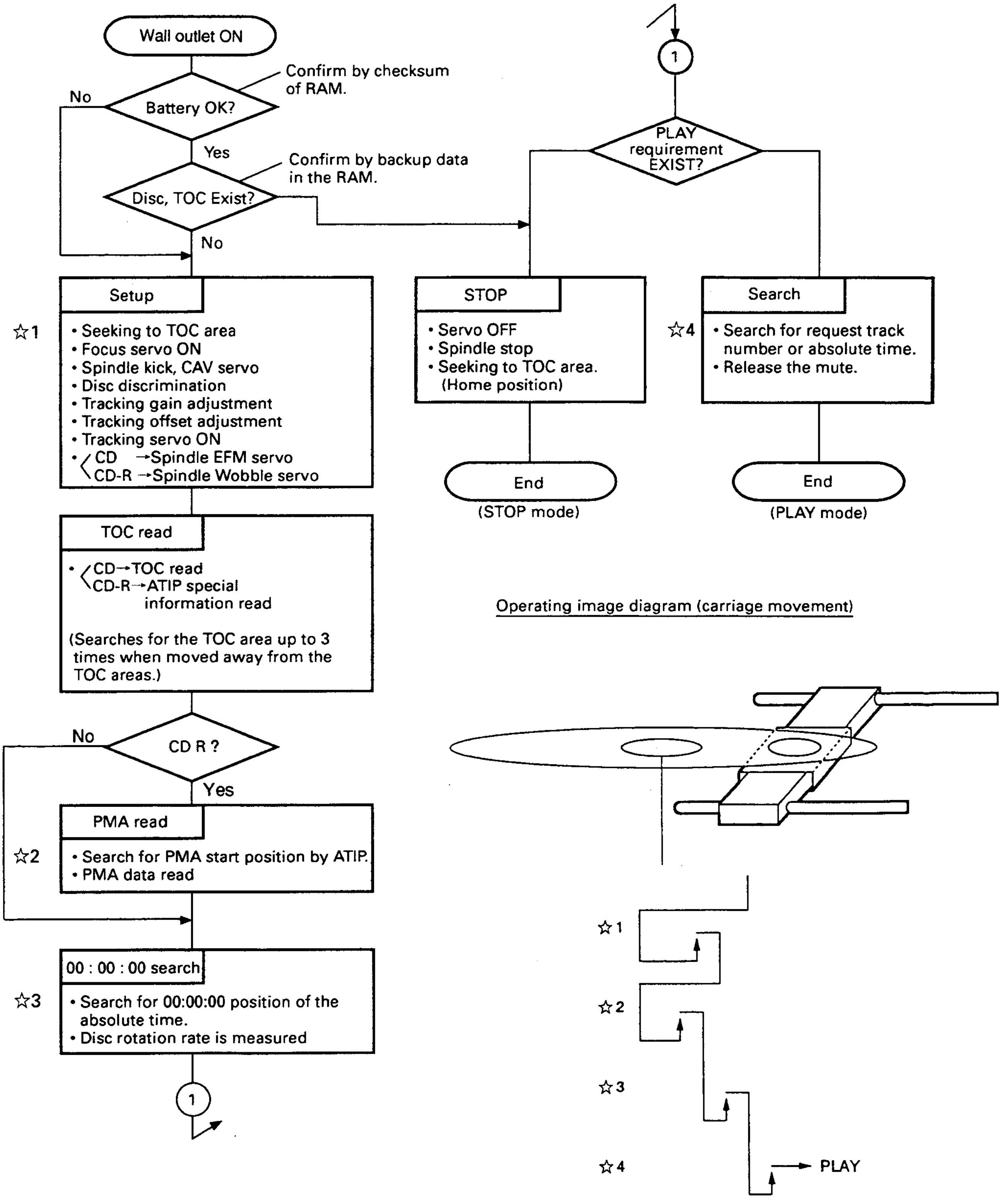
Pin No.	Mark	Name	I/O	Initial	Function
45	POA0	LDPW0	O	L	LSB
46	POA1	LDPW1	O	L	
47	POA2	LDPW2	O	L	5 bit (D/A out) recording laser power output setting
49	POA3	LDPW3	O	L	
50	POA4	LDPW4	O	L	MSB
51	POA5	SSEL	O	L	"L" when tracking error envelope detection is reset
52	POA6	—	O	L	Not used
53	POA7	LJUMP	O	L	"H" during N track jump
54	POB0	LIN	O	L	"H" during loading close
55	POB1	LOUT	O	L	"H" during loading open
56	POB2	KOJK	O	L	Optical axis switching circuit ON/OFF
57	POB3	EECS	O	L	EEPROM data writing and reading enable output
59	POB4	—	O	L	Not used
60	POB5	FC_OST	O	L	Focus offset switching output. During search: L. Other than search: H
61	POB6	—	O	L	Not used
62	POB7	—	O	L	
63	POC0	TEG0	O	L	LSB
64	POC1	TEG1	O	L	Tracking error amplifier gain adjustment
65	POC2	TEG2	O	L	
66	POC3	TEGM	O	L	MSB
67	POC4	DIRC	O	H	"L" when SONY servo IC DIRC is output
69	POC5	XCDMIR	O	H	Mirror detection circuit selection SW CD R/$\overline{\text{CD}}$
70	POC6	XLDON	O	H	Laser diode OFF/$\overline{\text{ON}}$
71	POC7	AMUTE	O	H	Audio final stage mute H (According to mode controller instructions) Turns mute ON during REC PAUSE, when input selector is switched, and during STOP

2. Peripheral Block Diagram (Servo Section)


ATIP decoder
IC207
PDJ006A
Addresses
8000-8FFF
DIRC (To servo LSI)
Audio final stage mute
Tracking error gain adjustment
TE envelope detection reset
Laser diode ON/OFF
Mirror detection circuit selection
Spindle STOP output
Recording laser power output
Loading open
Loading close
XCE0
XWR. XRD
A0-7
AD0-7
A12-14
A15
ATIP
RAM
IC352
Addresses 9000 to 9FFF
LH5116D-10 2 kbytes
XCE
A8-10
Address decoder
IC353
TC74HC573AP
Address
data bus
Address bus
Mechanism control
microprocessor
ASTB
XWR
XRD
IC356
PD4584A
RAME
Servo LSI
IC201
CXA1372Q
XLT, SENS
SSO, SSCK
Decorder LSI
IC206
CXD2500BQ
SSO
SSCK
XLT
SCOR
SENS
FG
SPSP
ECLV
CLV
RECE
ESYN
EXSC
OPEN
CLMP
XFUSE
MREQ
MACK
MSCK, MSI
MSO, XSUBQE
XENCE
XRESET
Spindle
circuit
Loading
mechanism
MSI
Serial bus SW
IC357
TC74HC367AP
Serial bus SW
IC358
TC74HC367AP
SQSO
SQCK
XFUSE
MREQ
MACK
MSO
MSCK
FSO, FSI
FSCK, LCE
XFUSE
DO
DI
CE
Mode control
microprocessor
IC351
PD4591A
IC301
PDC019A
(Audio digital board)
CD encoder LSI

3. Operating Flow Chart (1)

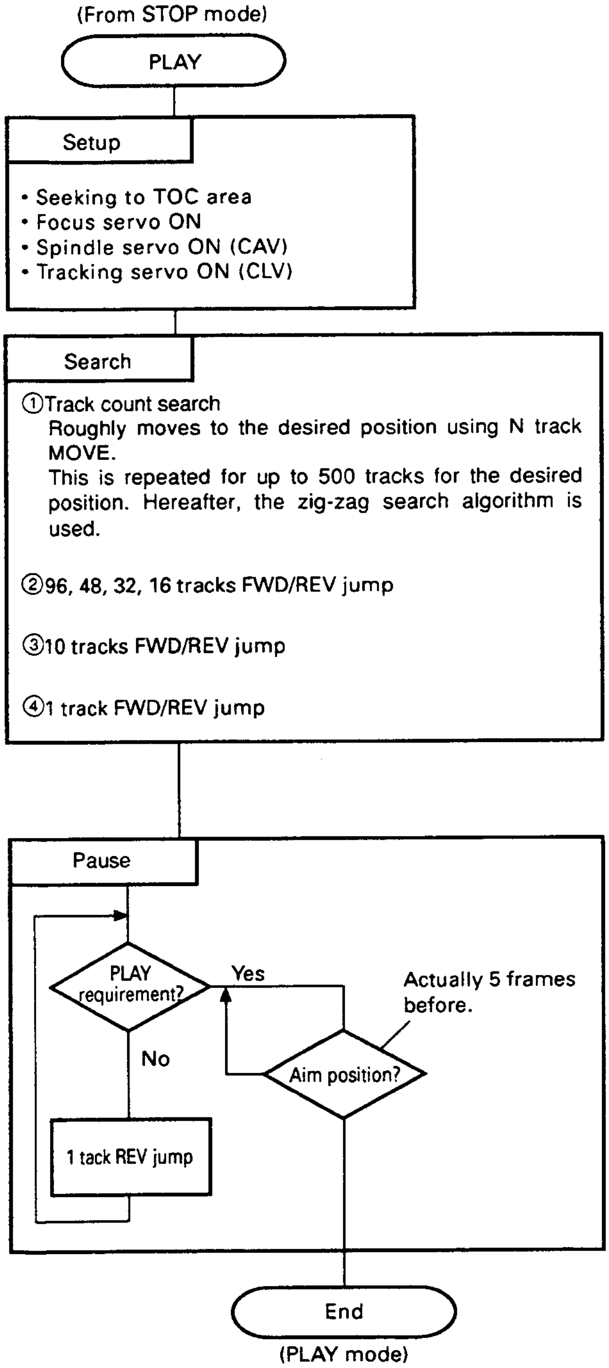
Wall outlet ON sequence


Wall outlet ON
Battery OK?
Confirm by checksum of RAM.
No
Yes
Disc, TOC Exist?
Confirm by backup data in the RAM.
No
Setup
☆1
• Seeking to TOC area
• Focus servo ON
• Spindle kick, CAV servo
• Disc discrimination
• Tracking gain adjustment
• Tracking offset adjustment
• Tracking servo ON
• CD →Spindle EFM servo
CD-R →Spindle Wobble servo
TOC read
• CD→TOC read
CD-R→ATIP special information read
(Searches for the TOC area up to 3 times when moved away from the TOC areas.)
CD R ?
No
Yes
PMA read
☆2
• Search for PMA start position by ATIP.
• PMA data read
00 : 00 : 00 search
☆3
• Search for 00:00:00 position of the absolute time.
• Disc rotation rate is measured
1
1
PLAY requirement EXIST?
STOP
• Servo OFF
• Spindle stop
• Seeking to TOC area. (Home position)
End
(STOP mode)
Search
☆4
• Search for request track number or absolute time.
• Release the mute.
End
(PLAY mode)
☆1
☆2
☆3
☆4
PLAY

Operating image diagram (carriage movement)

4. Operating Flow Chart (2)

STOP → PLAY sequence


(From STOP mode)
PLAY
Setup
Search
Pause
PLAY requirement?
Yes
No
1 tack REV jump
Aim position?
Actually 5 frames before.
End
(PLAY mode)

- Seeking to TOC area
- Focus servo ON
- Spindle servo ON (CAV)
- Tracking servo ON (CLV)

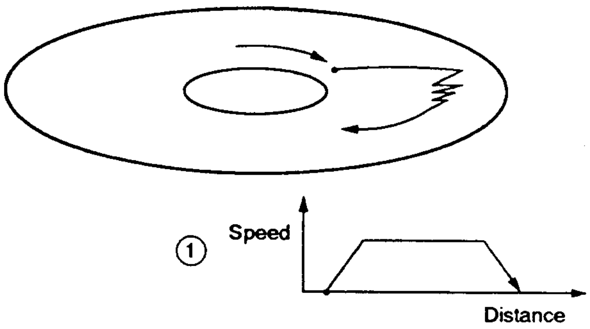
①Track count search
Roughly moves to the desired position using N track MOVE.
This is repeated for up to 500 tracks for the desired position. Hereafter, the zig-zag search algorithm is used.

②96, 48, 32, 16 tracks FWD/REV jump

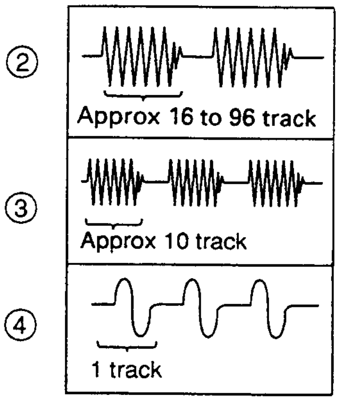
③10 tracks FWD/REV jump

④1 track FWD/REV jump

Operating image diagram

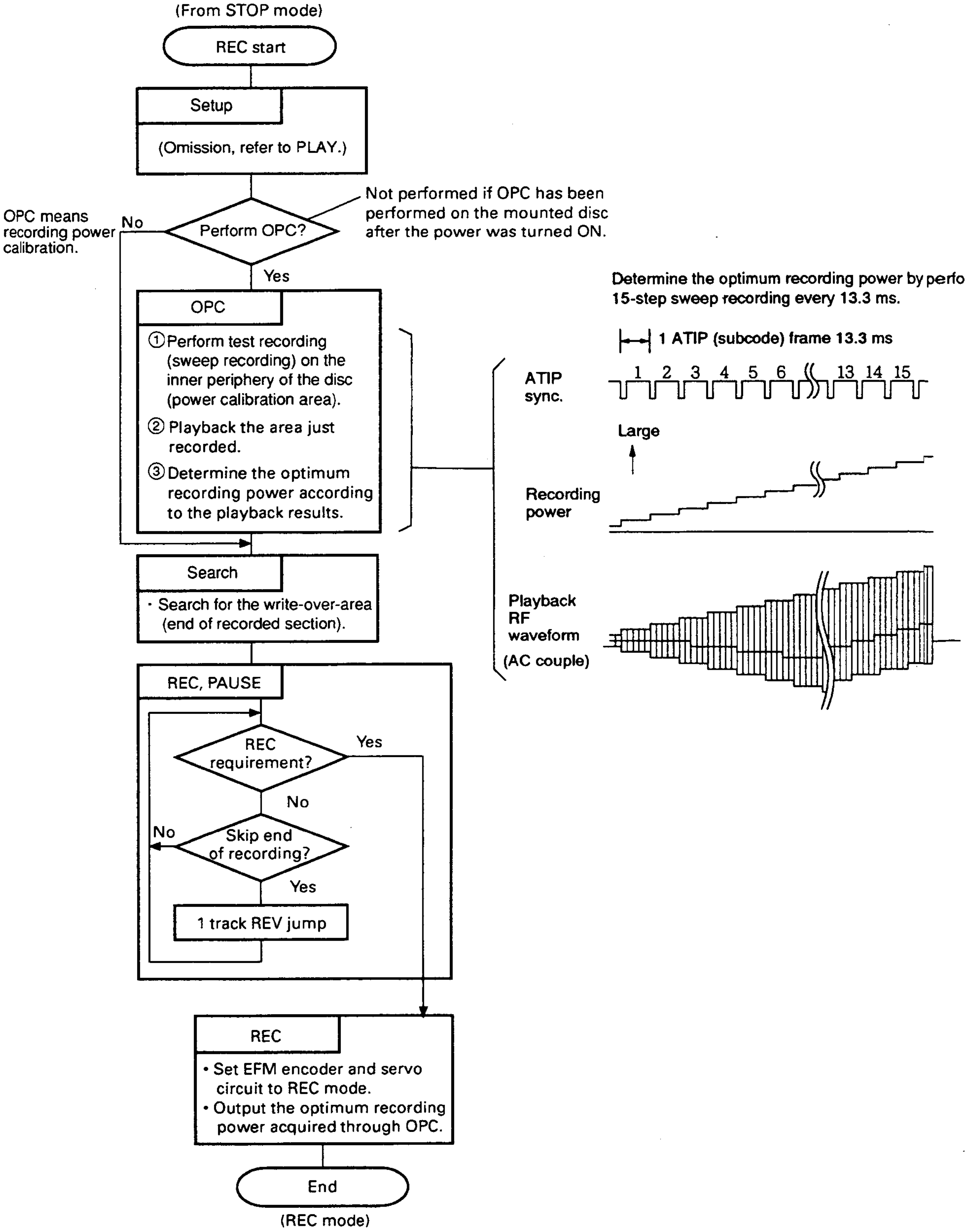

①
Speed
Distance

Tracking error waveforms


②
Approx 16 to 96 track
③
Approx 10 track
④
1 track

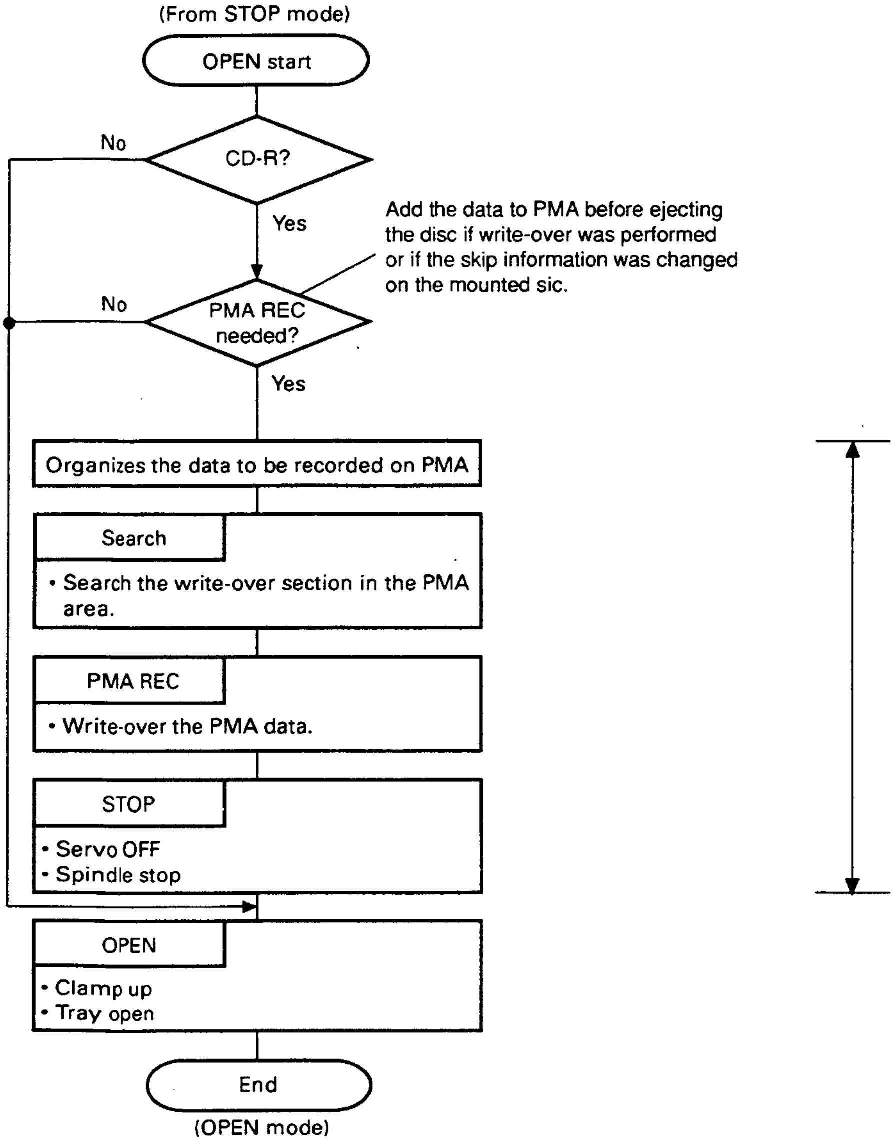
5. Operating Flow Chart (3)

STOP → REC sequence


(From STOP mode)
REC start
Setup
(Omission, refer to PLAY.)
Perform OPC?
Not performed if OPC has been performed on the mounted disc after the power was turned ON.
OPC means recording power calibration.
No
Yes
OPC
① Perform test recording (sweep recording) on the inner periphery of the disc (power calibration area).
② Playback the area just recorded.
③ Determine the optimum recording power according to the playback results.
Determine the optimum recording power by performing 15-step sweep recording every 13.3 ms.
1 ATIP (subcode) frame 13.3 ms
ATIP sync.
1
2
3
4
5
6
13
14
15
Large
Recording power
Playback RF waveform
(AC couple)
Search
· Search for the write-over-area (end of recorded section).
REC, PAUSE
REC requirement?
Yes
No
Skip end of recording?
No
Yes
1 track REV jump
REC
• Set EFM encoder and servo circuit to REC mode.
• Output the optimum recording power acquired through OPC.
End
(REC mode)

6. Operating Flow Chart (4)

STOP → OPEN sequence

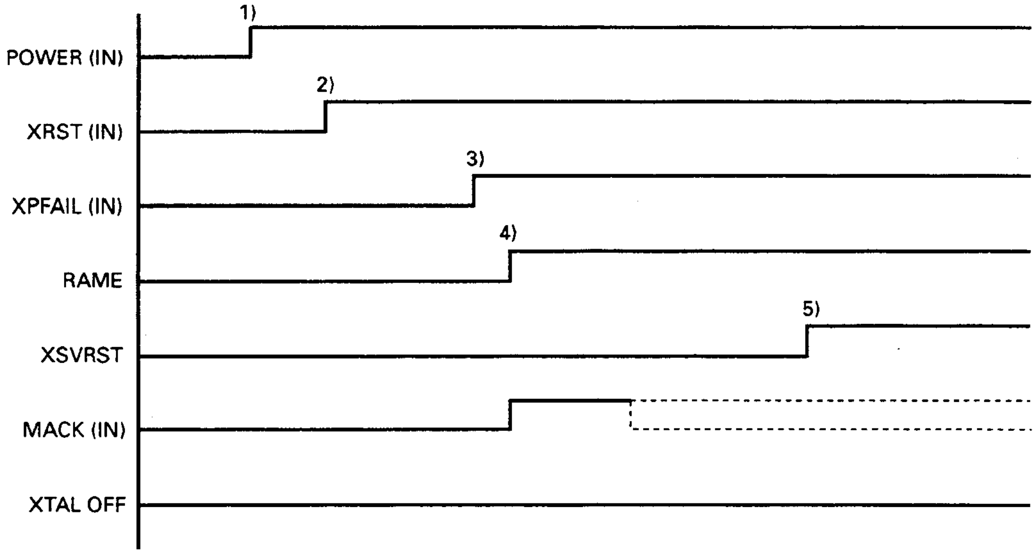

(From STOP mode)
OPEN start
CD-R?
No
Yes
PMA REC needed?
No
Yes
Organizes the data to be recorded on PMA
Search
• Search the write-over section in the PMA area.
PMA REC
• Write-over the PMA data.
STOP
• Servo OFF
• Spindle stop
OPEN
• Clamp up
• Tray open
End
(OPEN mode)
OPEN

Add the data to PMA before ejecting the disc if write-over was performed or if the skip information was changed on the mounted sic.

flashes on the display during these operations.

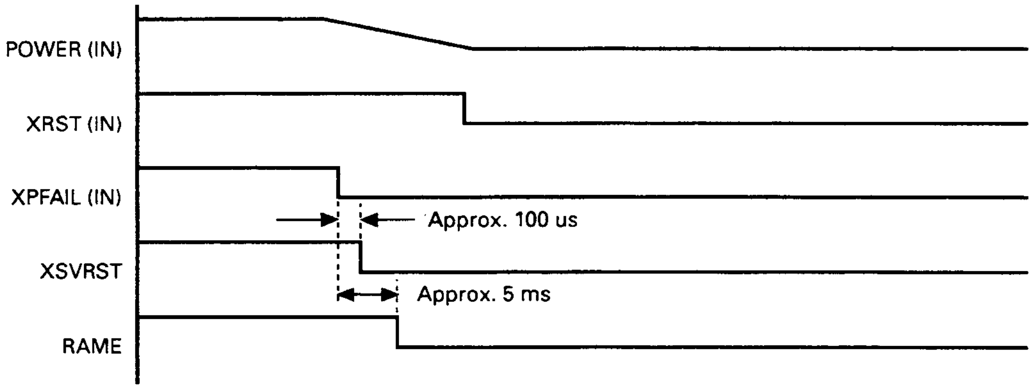
7. Timing Chart

① Timing Chart when Power On (Outlet On)


POWER (IN)
XRST (IN)
XPFAIL (IN)
RAME
XSVRST
MACK (IN)
XTAL OFF
1)
2)
3)
4)
5)

1) Power turns on.
2) XRST becomes H and reset is turned off.
3) After reset is turned off, wait for XPFAIL to become H.
4) After XPFAIL becomes H, the microprocessor starts.
RAME becomes H, and the external SRAM is set to the enable state.
5) XSVRST becomes H, and servo circuit operations start.

② Timing Chart when Power Failure

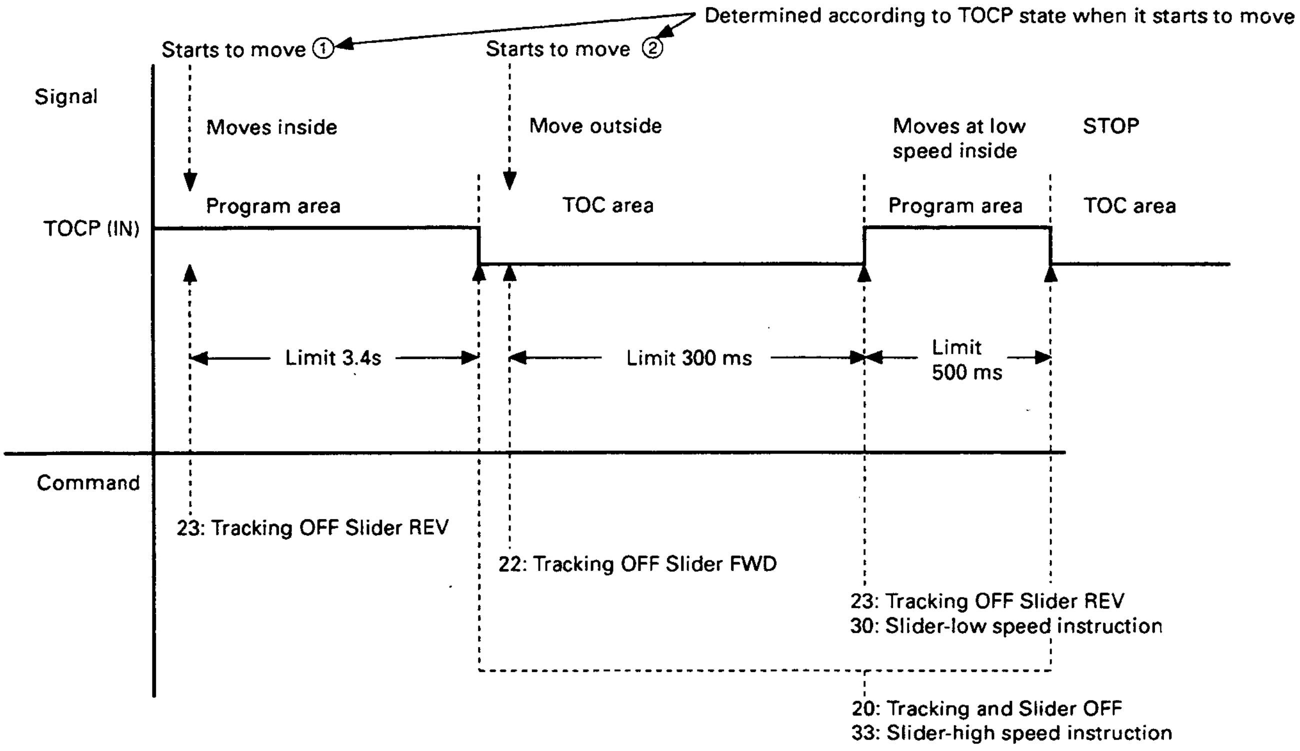

POWER (IN)
XRST (IN)
XPFAIL (IN)
Approx. 100 us
XSVRST
Approx. 5 ms
RAME

1) The power starts dropping and after a certain point, XPFAIL becomes L.
2) When XPFAIL becomes L, an internal interrupt is imposed, and the current operation mode and disc data are backed up.
3) At the same time, XSVRST becomes L, servo is reset, RAME is set to L, and the external SRAM is set to the disable state.
4) XRST then becomes L, and reset is set.

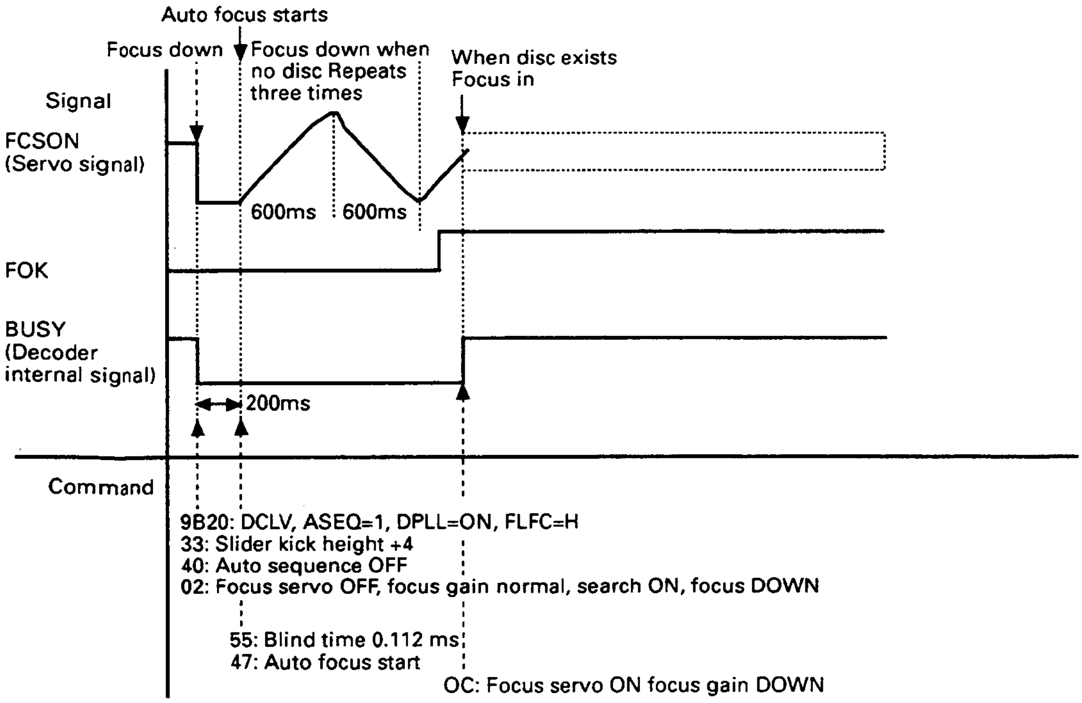
NOTE: If XRST becomes L first before RAME becomes L, the value of the backup RAM (IC352) will not be stored properly.

③ Seek Track 0

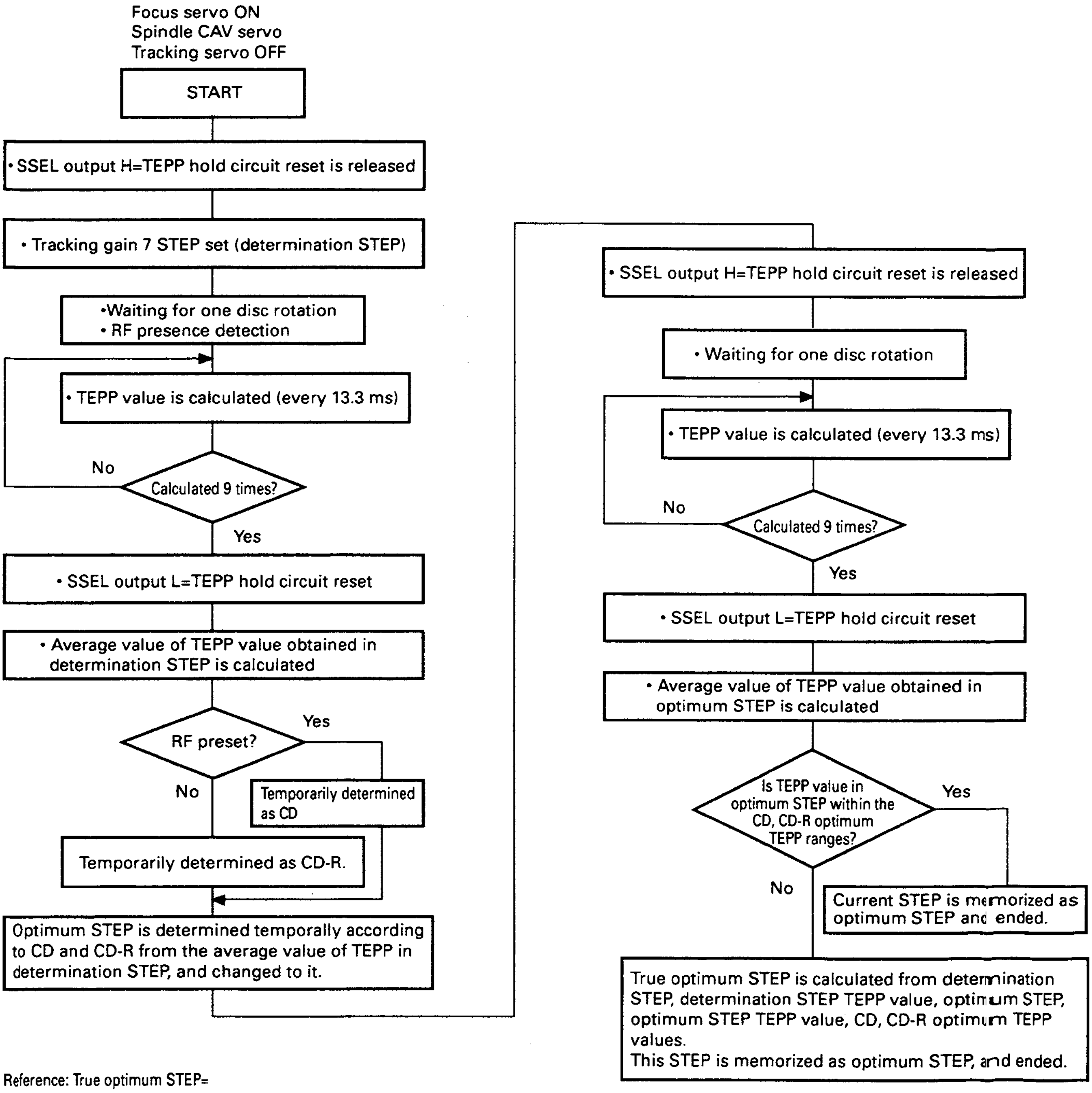
Carriage is moved to TOC area (Home position).


Determined according to TOCP state when it starts to move
Starts to move ①
Starts to move ②
Signal
Moves inside
Move outside
Moves at low speed inside
STOP
TOCP (IN)
Program area
TOC area
Program area
TOC area
Limit 3.4s
Limit 300 ms
Limit 500 ms
Command
23: Tracking OFF Slider REV
22: Tracking OFF Slider FWD
23: Tracking OFF Slider REV
30: Slider-low speed instruction
20: Tracking and Slider OFF
33: Slider-high speed instruction

④ Focus ON


Auto focus starts
Focus down
Focus down when no disc Repeats three times
When disc exists Focus in
Signal
FCSON (Servo signal)
600ms
600ms
FOK
BUSY (Decoder internal signal)
200ms
Command
9B20: DCLV, ASEQ=1, DPLL=ON, FLFC=H
33: Slider kick height +4
40: Auto sequence OFF
02: Focus servo OFF, focus gain normal, search ON, focus DOWN
55: Blind time 0.112 ms
47: Auto focus start
OC: Focus servo ON focus gain DOWN

8. Tracking Error Gain Adjustment Flow Chart


Focus servo ON
Spindle CAV servo
Tracking servo OFF
START
• SSEL output H=TEPP hold circuit reset is released
• Tracking gain 7 STEP set (determination STEP)
•Waiting for one disc rotation
• RF presence detection
• TEPP value is calculated (every 13.3 ms)
No
Calculated 9 times?
Yes
• SSEL output L=TEPP hold circuit reset
• Average value of TEPP value obtained in determination STEP is calculated
RF preset?
Yes
No
Temporarily determined as CD
Temporarily determined as CD-R.
Optimum STEP is determined temporally according to CD and CD-R from the average value of TEPP in determination STEP, and changed to it.
• SSEL output H=TEPP hold circuit reset is released
• Waiting for one disc rotation
• TEPP value is calculated (every 13.3 ms)
No
Calculated 9 times?
Yes
• SSEL output L=TEPP hold circuit reset
• Average value of TEPP value obtained in optimum STEP is calculated
Is TEPP value in optimum STEP within the CD, CD-R optimum TEPP ranges?
Yes
No
Current STEP is memorized as optimum STEP and ended.
True optimum STEP is calculated from determination STEP, determination STEP TEPP value, optimum STEP, optimum STEP TEPP value, CD, CD-R optimum TEPP values.
This STEP is memorized as optimum STEP, and ended.

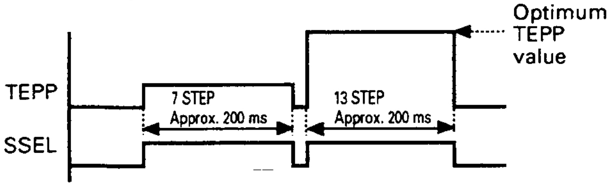
Reference: True optimum STEP=

$$= \frac{\text{Determination STEP} - \text{Optimum STEP}}{\text{TEPP value of determination STEP} - \text{Optimum STEP TEPP value}} (\text{CD, CD-R optimum TEPP value} - \text{optimum STEP TEPP value}) + \text{Optimum STEP}$$

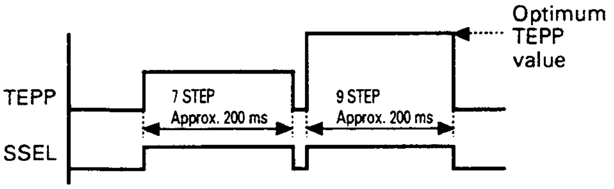
9. Tracking Gain Adjustment Timing Chart

CD Optimum TEPP value : 2.26V ±0.103V (2.157 to 2.372V)
CD-R Optimum TEPP value : 2.494V ±0.103V (2.372 to 2.649V)

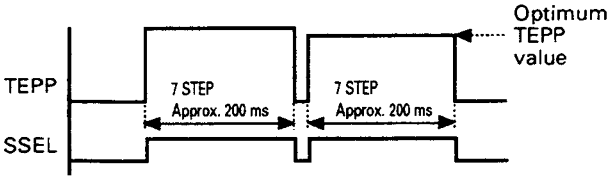
1) Example of increasing gain to maximum after disc gain became low


Optimum TEPP value
TEPP
SSEL
7 STEP
Approx. 200 ms
13 STEP
Approx. 200 ms

2) Example of increasing gain after disc gain became low


Optimum TEPP value
TEPP
SSEL
7 STEP
Approx. 200 ms
9 STEP
Approx. 200 ms

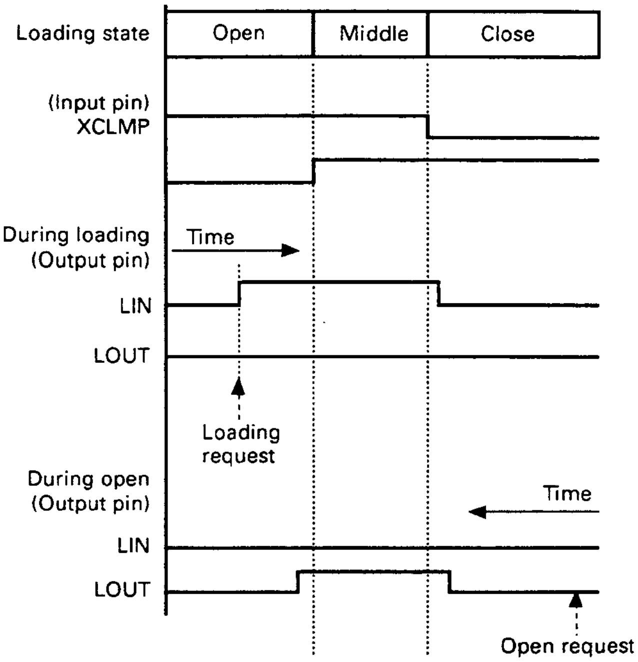
3) Example of decreasing gain to minimum after disc gain became high


Optimum TEPP value
TEPP
SSEL
7 STEP
Approx. 200 ms
7 STEP
Approx. 200 ms

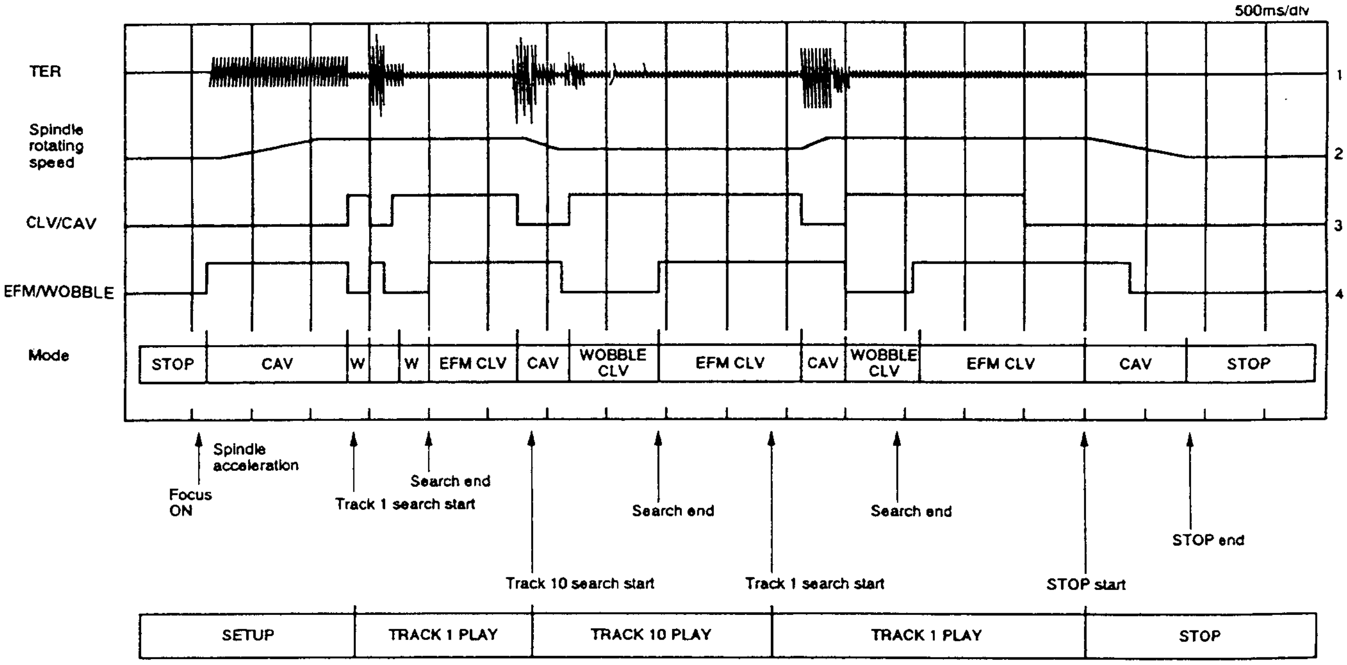
10. Loading Control for Turn Table

Open/Close Control and SW States

The following shows the timing chart of the loading-related input/output pins.


Loading state
Open
Middle
Close
(Input pin)
XCLMP
During loading
(Output pin)
Time
LIN
LOUT
Loading request
During open
(Output pin)
Time
LIN
LOUT
Open request

11. Spindle Servo Mode Selection during CD-R, STOP→PLAY→Search→STOP Operations



■ PD4591A (SERVO UCOM BOARD ASSY, IC351)
Mode Control Microcomputer

● Pin Function

Pin No.	Mark	Name	I/O	Initial	Function
1	FIP6	GRID 6	O	L	FL grid output 5
2	FIP5	GRID 5	O	L	FL grid output 6
3	FIP4	GRID 4	O	L	FL grid output 7
4	FIP3	GRID 3	O	L	FL grid output 8
5	FIP2	GRID 2	O	L	FL grid output 9
6	FIP1	GRID 1	O	L	FL grid output 10
7	FIP0	GRID 0	O	L	FL grid output 11
8	VDD	VDD	O	L	Connected to VDD
9	SCK0	RSCK	O	H	Not used
10	SO0	RSO	O	L	
11	SI0	RSI	I	—	
12	P24	RACK	O	L	
13	P23	RREQ	O	L	
14	SCK1	FSCK	I/O	H	Mechanism controller, LSI serial clock
15	SO1	FSO	O	L	Mechanism controller, serial output
16	SI1	FSI	I	—	Mechanism controller, serial input
17	RESET	XRESET	I	L	Mode controller reset input
18	P74	LED4	O	H	Display ON/OFF LED (L: LED ON)
19	P73	LED3	O	H	Standby LED (L: LED ON)
20	AVSS	GND	I	—	Connected to GND
21	P17	XFUSE	O	H	Mode controller serial communication currently used (L)
22	P16	—	O	L	Not used
23	P15	FSLAT	O	H	CE for PDC020A. L: Select
24	P14	XTALOFF	O	L	XTAL ON (L), OFF (H)
25	P13	XEMP	O	H	Emphasis control. L: deemphasis
26	P12	XRST	O	L	Mechanism controller, ATIP decoder reset
27	P11	—	O	L	Not used
28	P10	—	O	L	
29	AVDD	VDD	—	—	Connected to VDD
30	AVREF	VDD	—	—	
31	P04	MODE	I	—	Not used. L: Fixed
32	XT2	—	O	—	Not used
33	VSS	GND	—	—	Connected to GND
34	X1	—	I	—	System oscillation 4.19MHz
35	X2	—	O	—	
36	P37	SW1	I	L	Mode ON/OFF (L: Fixed)
37	P36	DIP1	O	L	Not used
38	P35	DIP2	O	L	
39	P34	DIP3	O	L	
40	P33	DIP4	O	L	

Note) U: Pull-up, D: Pull-down

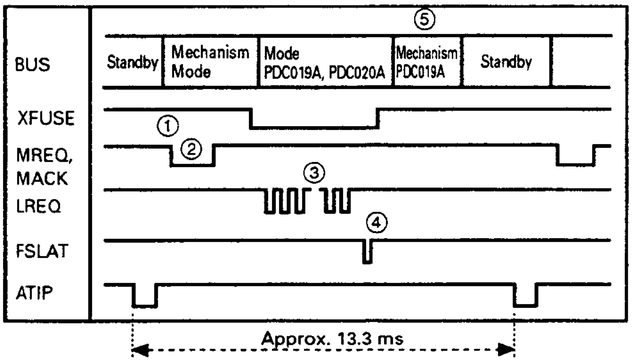
Pin No.	Mark	Name	I/O	Initial	Function
41	P32	MACK	O	H	Mechanism controller communication response
42	P31	LREQ	O	H	PDC019A CE signal
43	P30	UNLOCK	I	—	Digital unlock detection
44	INTP3	DIGOUT	I	—	Digital output ON/OFF. (H: DIGITAL OUTPUT ON)
45	INTP2	XPFAIL	I	—	Power down detection. L:Power down
46	INTP1	MREQ	I	—	Mechanism controller communication request (Interrupt)
47	INTP0	REMIN	I	—	Remote control input (Interrupt)
48	IC	VPP	I	—	Connected to GND
49	P72	LED2	O	L	Not used
50	P71	LED1	O	H	REC indicator LED (L: LED ON)
51	P70	LED0	O	H	Manual track increment enable (L: LED ON)
52	VDD	VDD	—	—	Connected to VDD
53	P127	SCAN4	O	L	Key matrix output 4
54	P126	SCAN3	O	L	Key matrix output 3
55	P125	SCAN2	O	L	Key matrix output 2
56	P124	SCAN1	O	L	Key matrix output 1
57	P123	SCAN0	O	L	Key matrix output 0
58	P122	KEYIN3	I	—	Key matrix input 3
59	P121	KEYIN2	I	—	Key matrix input 2
60	P120	KEYIN1	I	—	Key matrix input 1
61	P117	KEYIN0	I	—	Key matrix input 0 (Including test SW)
62	P116	—	O	L	Not used
63	P115	—	O	L	
64	P114	—	O	L	
65	P113	SEG 10	O	L	FL segment output 10
66	P112	SEG 9	O	L	FL segment output 9
67	P111	SEG 8	O	L	FL segment output 8
68	P110	SEG 7	O	L	FL segment output 7
69	P107	SEG 6	O	L	FL segment output 6
70	P106	SEG 5	O	L	FL segment output 5
71	VLOAD	VLOAD	—	—	VLOAD
72	P105	SEG 4	O	L	FL segment output 4
73	P104	SEG 3	O	L	FL segment output 3
74	P103	SEG 2	O	L	FL segment output 2
75	P102	SEG 1	O	L	FL segment output 1
76	P101	SEG 0	O	L	FL segment output 0
77	P100	GRID 10	O	L	FL grid output 10
78	FIP9	GRID 9	O	L	FL grid output 9
79	FIP8	GRID 8	O	L	FL grid output 8
80	FIP7	GRID 7	O	L	FL grid output 7

1. System serial communication

The mode controller performed serial communication between the mechanism controller and PDC019A (digital interface LSI) and PDC020A (FS converter LSI).

The mechanism controller also performed communication with PDC019A at the following timings.

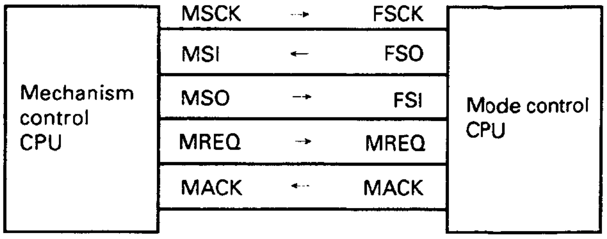
①Communication request from mechanism controller.
②Mechanism/mode controller communication
③Communication with mode controller/PDC019A
During this time, XFUSE is set to L and serial communication of mechanism controller is disabled.
④Serial communication with mode controller/PDC020A
⑤Communication with mechanism controller/PDC019A


⑤
BUS
Standby
Mechanism Mode
Mode PDC019A, PDC020A
Mechanism PDC019A
Standby
XFUSE
①
MREQ, MACK
②
③
LREQ
④
FSLAT
ATIP
Approx. 13.3 ms

2. Communication with Mechanism Controller and Mode Controller

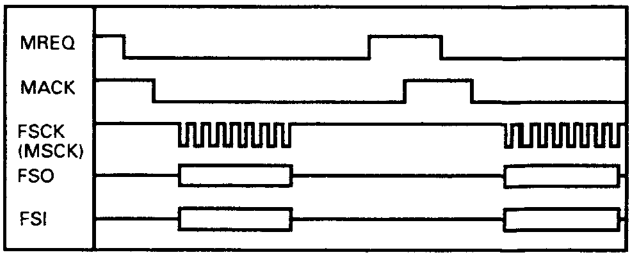
Communication Format

This CPU and the mechanism control CPU performed serial communication with 5 signal lines.


Mechanism control CPU
MSCK → FSCK
MSI ← FSO
MSO → FSI
MREQ → MREQ
MACK ← MACK
Mode control CPU

- ● FSCK .... Serial transmission clock (1 MHz)
- ● FSI/FSO .... Serial data transmission line
- ● MREQ/MACK ...... Handshake line

The communication timing is control by the mechanism control CPU. 13 byte data is transmitted every 13.33 to 40 ms. (Average:13.33 msec)


MREQ
MACK
FSCK (MSCK)
FSO
FSI

Communication is performed by the following procedure.

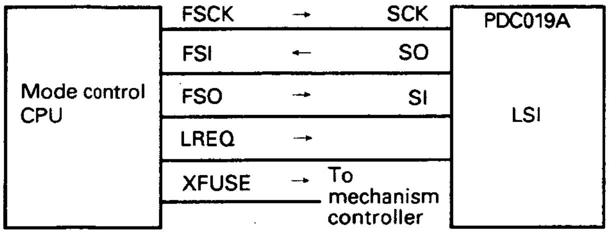
①The MREQ signal becomes L as communication request from the mechanism control microprocessor.
②This microprocessor sets the MACK signal to L as communication enable signal.
③The mechanism controller sets the MREQ signal to H after 1 byte serial transmission.
④This microprocessor sets MACK to H if serial transmission has ended normally.
⑤Hereafter ① to ④ are repeated until the 13 byte data transmission has completed.
※The mechanism controller and mode controller observes the state of the other side's control line, and stops communication processing of transmission if conditions are not satisfied after a certain time.

3. Communication with digital interface LSI (PDC019A, IC301)

Communication format

Communication with the digital interface LSI is performed using four lines.

XFUSE is set to L during communication so that there are no clashes with the mechanism controller.


Mode control CPU
FSCK → SCK
FSI ← SO
FSO → SI
LREQ →
XFUSE → To mechanism controller
PDC019A
LSI

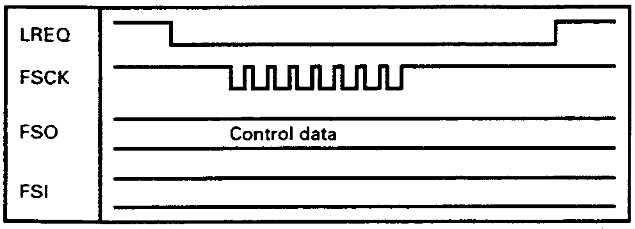
- ●FSCK .... Serial transmission clock (1 MHz)
- ●FSI/FSO .... Serial data transmission line
- ●BLREQ........... Data enable
- ●XFUSE .... L when the mode controller is using the communication line

Communication is performed in one main routine.

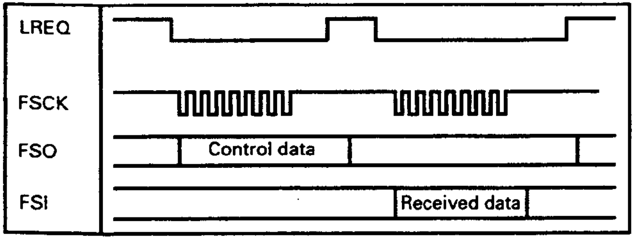
The communication timing is controlled by the mode controller.

No transmission is performed during communication between the mechanism controller and PDC019A.

(Command control)


LREQ
FSCK
FSO
Control data
FSI

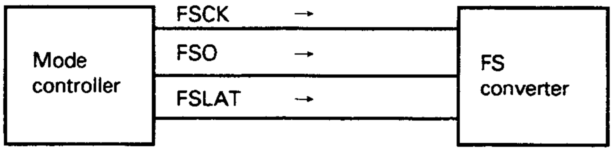
(Data reading)


LREQ
FSCK
FSO
Control data
FSI
Received data

4. fs Converter Control

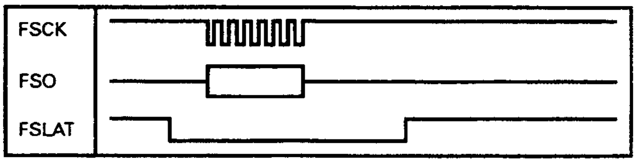
Communication is performed by 1 byte transmission only in one direction from the microprocessor to fs converter (PDC020A, IC306).

The communication format is as follows.


Mode controller
FSCK →
FSO →
FSLAT →
FS converter

- ● FSCK .... Serial transmission clock (1 MHz)
- ● FSO .... Serial data transmission line
- ● FSLAT .... fs converter communication enable signal

1 byte is transmitted after communication with the PDC019A LSI.

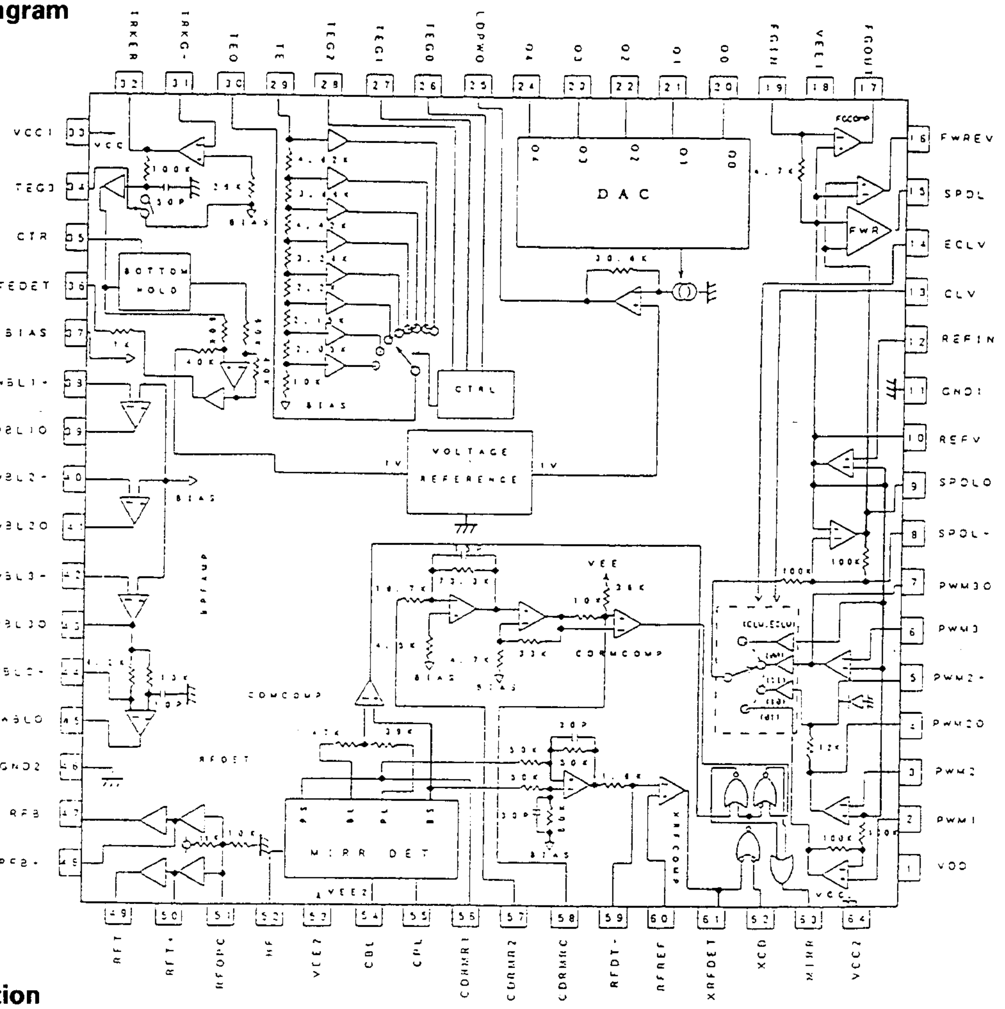

FSCK
FSO
FSLAT

The data obtained by communication is 1 byte of LSB first.

Bit	Name	Initial	Function
D0	MKSEL	L	L: 384fs, H: 512fs
D1	FSEL1	L	L: 44.1k
D2	FSEL2	L	When FSEL=1 L: 48k, H: 32k
D3	MUTE	L	L: OFF, H: Mute
D4	STOP VCO	L	L: PLL transmission stop, H: PLL transmission VCO ON/OFF (H: ON) (Used together)
D5	XOPTSW	H	OPT SW ON/OFF (L: ON)
D6	XENVCO	H	VCO for PDC019A ON/OFF (L: ON)
D7	XTALSEL	H	Crystal select (H: XTAL)

■ PA9004A (SERVO UCOM BOARD ASSY, IC205) CDR SERVO AMP

● Block Diagram


TRKER 32
TRKG- 31
TEO 30
TE 29
TEG2 28
TEG1 27
TEG0 26
LDPWO 25
O4 24
O3 23
O2 22
O1 21
O0 20
FGIN 19
VEE1 18
FGOUT 17
FWREV 16
SPDL 15
ECLV 14
CLV 13
REFIN 12
GND1 11
REFV 10
SPDLO 9
SPDL- 8
PWM3O 7
PWM3 6
PWM2+ 5
PWM2O 4
PWM2 3
PWM1 2
VDD 1
VCC1 33
TEG3 34
CTR 35
TEDET 36
BIAS 37
WBL1- 38
WBL1O 39
WBL2- 40
WBL2O 41
WBL3- 42
WBL3O 43
ABL- 44
ABLO 45
GND2 46
RFB 47
RFB- 48
RFT 49
RFT+ 50
RFOPC 51
HF 52
VEE2 53
CBL 54
CPL 55
CDRMR1 56
CDRMR2 57
CDRMRC 58
RFDT- 59
RFREF 60
XRFDET 61
XCD 62
MIRR 63
VCC2 64
DAC
CTRL
VOLTAGE REFERENCE
BOTTOM HOLD
MIRR DET
FCCOMP
FWR
CDRMCOMP
BIAS
VCC

● Pin Function

Pin No.	Name	I/O	Function
1	VDD	–	+5V power supply pin
2	PWM1	I	CAV PWM rectification amplifier input pin
3	PWM2	I	WOBBLE CLV rectification amplifier input pin
4	PWM2O	O	WOBBLE CLV rectification amplifier output pin
5	PWM2+	I	WOBBLE CLV LPF capacity connection pin
6	PWM3	I	EFM CLV rectification amplifier input pin
7	PWM3O	O	EFM CLV rectification amplifier output pin
8	SPDL–	I	Amplifier inversion input pin for spindle motor with brush
9	SPDLO	O	Amplifier output pin for spindle motor with brush
10	REFV	O	Spindle reference voltage output pin
11	GND1	–	Ground pin
12	REFIN	I	Spindle reference voltage input pin
13	CLV	I	Spindle control mode setting signal input pin
14	ECLV	I	
15	SPDL	O	Brushless spindle motor amplifier output pin

MODE	STOP	CAV	WOBBLECLV	FEMCLV
CLV	L	L	H	H
ECLV	L	H	L	H

Pin No.	Name	I/O	Function
16	FWREV	O	Brushless spindle motor polarity signal output pin
17	FGOUT	O	FG comparator output pin
18	VEE1	–	–4V power supply pin
19	FGIN	I	FG comparator input pin
20	Q0	I	DA converter data input pin for setting LD power
21	Q1	I	
22	Q2	I	
23	Q3	I	
24	Q4	I	
25	LDPWO	O	Voltage output pin for setting LD power
26	TEG0	I	Data input pin for setting tracking error gain
27	TEG1	I	
28	TEG2	I	
29	TE	I	Tracking error signal input pin
30	TEO	O	Amplifier output pin for setting tracking error gain
31	TRKG–	I	Tracking error amplifier inversion input pin
32	TRKER	O	Tracking error amplifier output pin
33	VCC1	–	+4V power supply pin
34	TEG3	I	Tracking error signal level detection mute signal input pin
35	CTR	I	Hold capacitor connection pin for level detection
36	TEDET	O	Tracking error signal level detection signal output pin
37	BIAS	I	Ground pin
38	WBL1–	I	WOBBLE BPF amplifier 1 inversion input pin
39	WBL1O	O	WOBBLE BPF amplifier 1 output pin
40	WBL2–	I	WOBBLE BPF amplifier 2 inversion input pin
41	WBL2O	O	WOBBLE BPF amplifier 2 output pin
42	WBL3–	I	WOBBLE BPF amplifier 3 inversion input pin
43	WBL3O	O	WOBBLE BPF amplifier 3 output pin
44	WBLC–	I	WOBBLE comparator inversion input pin
45	WBLO	O	WOBBLE comparator output pin
46	GND2	–	Ground pin
47	RFB	O	OPC RF bottom level detection signal output pin
48	RFB+	I	OPC RF bottom level detection time-constant setting pin
49	RFT	O	OPC RF top level detection signal output pin
50	RFT+	I	OPC RF top level detection time-constant setting pin
51	RFOPC	I	OPC RF signal input pin
52	HF	I	Mirror detection HF signal input pin
53	VEE2	–	–4V power supply pin
54	CBL	I	Mirror detection bottom hold capacity connection pin
55	CPL	I	Mirror detection peak hold capacity connection pin
56	CDRMR1	O	CDR mirror detection signal output pin
57	CDRMR2	I	CDR mirror detection signal input pin
58	CDRMRC	I	CDR mirror comparator non-inversion input pin
59	RFDT–	I	RF detection comparator inversion input pin
60	RFREF	I	RF detection comparator non-inversion input pin
61	RFDET	O	RF detection signal output pin
62	XCD	I	Mirror selection signal input pin
63	MIRR	O	Mirror signal output pin
64	VCC2	–	+4V power supply pin

■ PDJ006A (SERVO UCOM BOARD ASSY, IC207)
ATIP DECODER

● Pin Function

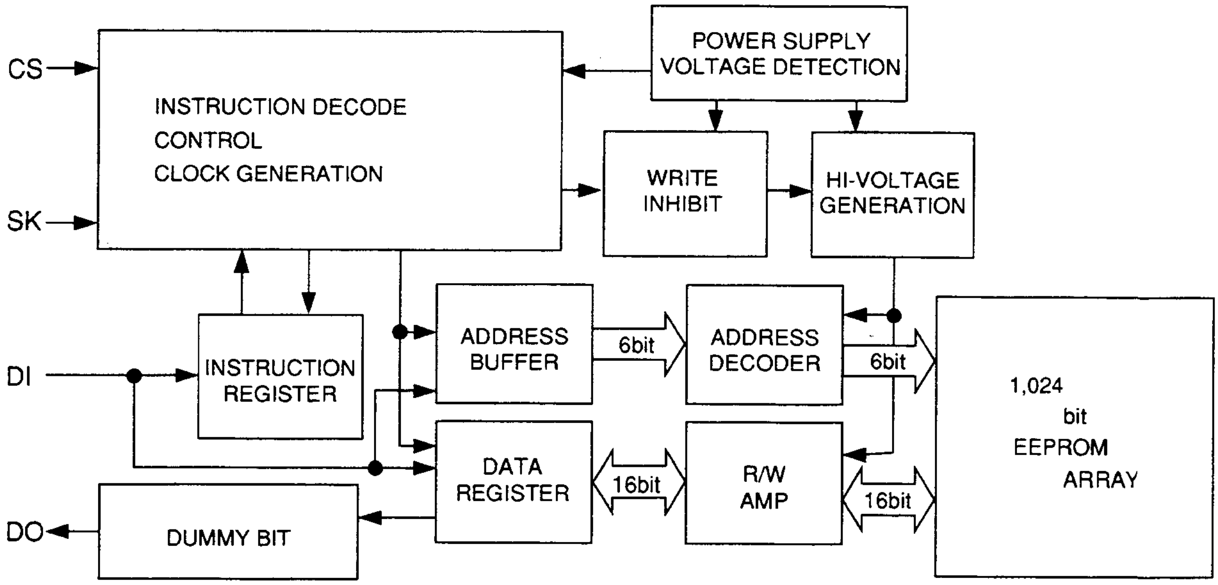
Pin No.	Name	I/O	Function
1	WBL	I	WOBBLE signal input pin
2	FSK	O	FSK demodulation signal output pin
3	SBSY	I	Subcode sync signal input pin
4	MDP	O	CLV servo MDP output pin
5	SPSEL	I	CPU interface mode selection signal input pin. H : Serial. L : Parallel
6	ASYNC	O	ATIP sync output pin
7	ACK	I	Serial interface clock input pin
8	GND	–	Ground pin
9	AOUTPE	I	Serial mode data read enable input pin
10	AOUT	O	Serial mode data output pin
11	AINPE	I	Serial mode data write enable input pin
12	AIN	I	Serial mode data input pin
13	XCK	I	Master clock input pin
14	XSRST	I	System reset input pin. L : reset
15	SIOK	O	Special information standby flag output pin. H: Special information readable. L : Not readable
16	CRCOK	O	CRC calculation results output pin. H : CRCOK. L : CRCNG
17	RPOTECT	O	ATIP sync protection state output pin. H : Protected. L : Not protected.
18	VCC	–	+5V power supply pin
19	N. C.	–	Not connected
20	XADSEL	I	Address decoder start address setting strobe input pin
21	XWE	I	Parallel mode data write enable input pin
22	XRE	I	Parallel mode data read enable input pin
23	SYA0	I	Parallel mode address bus input pin
24	SYA1	I	
25	SYA2	I	
26	SYA3	I	
27	SYA12	I	
28	GND	–	Ground pin
29	SYA13	I	Parallel mode address bus input pin
30	SYA14	I	
31	SYA15	I	
32	SYD0	I/O	Parallel mode data bus input/output pin
33	SYD1	I/O	
34	SYD2	I/O	
35	SYD3	I/O	
36	SYD4	I/O	
37	SYD5	I/O	
38	VCC	–	+5V power supply pin
39	SYD6	I/O	Parallel mode data bus input/output pin
40	SYD7	I/O	

Pin No.	Name	I/O	Function
41	XCE0	O	Chip select output pin
42	XCE1	O	
43	XCE2	O	
44	XCE3	O	
45	POA0	I/O	General register A parallel output pin
46	POA1	I/O	
47	POA2	I/O	
48	GND	–	Ground pin
49	POA3	I/O	General register A parallel output pin
50	POA4	I/O	
51	POA5	I/O	
52	POA6	I/O	
53	POA7	I/O	
54	POB0	O	General register B parallel output pin
55	POB1	O	
56	POB2	O	
57	POB3	O	
58	VCC	–	+5V power supply pin
59	POB4	O	General register B parallel output pin
60	POB5	O	
61	POB6	O	
62	POB7	O	
63	POC0	O	General register C parallel output pin
64	POC1	O	
65	POC2	O	
66	POC3	O	
67	POC4	O	
68	GND	–	Ground pin
69	POC5	O	General register C parallel output pin
70	POC6	O	
71	POC7	O	
72	TESTB	I	For tests
73	TEST	I	
74	TEST0	I	
75	TEST1	I	
76	TEST2	I	
77	TEST3	I	
78	VCC	–	+5V power supply pin
79	TEST4	I	For tests
80	N. C.	–	Not connected

■ (SERVO UCOM BOARD ASSY, IC360)

64×16 BIT EEPROM

● Block Diagram


CS
SK
DI
DO
INSTRUCTION DECODE
CONTROL
CLOCK GENERATION
POWER SUPPLY
VOLTAGE DETECTION
WRITE
INHIBIT
HI-VOLTAGE
GENERATION
INSTRUCTION
REGISTER
ADDRESS
BUFFER
6bit
ADDRESS
DECODER
6bit
1,024
bit
EEPROM
ARRAY
DATA
REGISTER
16bit
R/W
AMP
16bit
DUMMY BIT

● Pin Function

Pin No.	Name	I/O	Function
1	N. C.	–	Not connected
2	Vcc	–	Power supply pin
3	CS	I	Chip select input pin
4	SK	I	Serial clock input pin
5	DI	I	Start bit, ope-code, address, serial data input pin
6	DO	O	Serial data output. READY/XBUSY internal state display output
7	GND	–	Ground pin
8	N. C.	–	Not connected

■ PDC020A (AUDIO DIGITAL BOARD ASSY, IC306)
FS CONVERTER

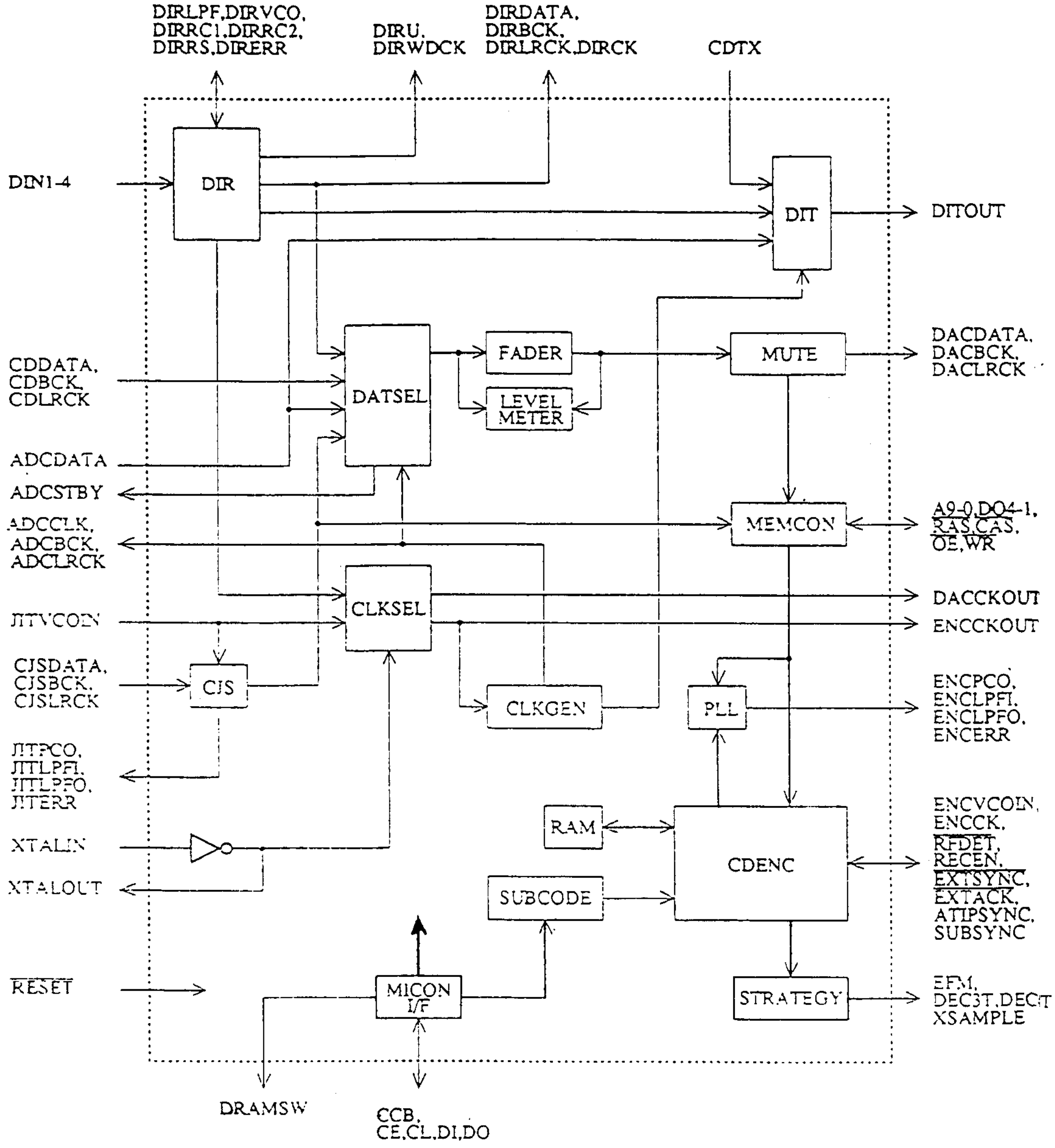
● Pin Function

Pin No.	Name	I/O	Function
1	MKSEL	I	Digital filter master clock selection signal input pin. H : 512fs L : 384 fs
2	INITB	I	System reset input pin. L : Reset
3	MCK1	I	Digital filter master clock input pin
4	BCLKI	I	Bit clock input pin
5	WCLKI	I	Word clock input pin
6	DGND	–	Ground pin
7	DVDD	–	+5V power supply pin
8	LRCKI	I	LR clock input pin
9	DATAI	I	Audio data input pin
10	CCB	I	CPU interface method selection signal input pin. H : Sanyo CCB format. L : General serial format
11	SPSEL	I	Mode setting selection signal input pin. H:Parallel. L:Serial
12	CE	I	CPU interface chip enable signal input pin
13	CL	I	CPU interface data transfer clock input pin
14	DI	I	CPU interface data input pin
15	DO7	O	CPU interface input data serial/parallel conversion output pin
16	DO6	O	
17	DO5	O	
18	DGND	–	Ground pin
19	DVDD	–	+5V power supply pin
20	DO4	O	CPU interface input data serial/parallel conversion output pin
21	DO3	O	
22	DO2	O	
23	DO1	O	
24	DO0	O	
25	DATAO	O	Audio data output pin
26	LRCKO	O	LR clock output pin
27	WCLKO	O	Word clock output pin
28	BCLKO	O	Bit clock output pin
29	DGND	–	Ground pin
30	N. C.	–	Not connected
31	AGND	–	Analog ground pin
32	VCO	O	PLL low pass filter pin
33	VIN	I	VCO freerunning oscillation setting input pin
34	R	I	VCO oscillation band adjustment input pin
35	STOP	I	VCO oscillation stop signal input pin. H : Oscillation. L : Oscillation stops
36	UNLK	O	Lock state monitor signal output pin. H : Unlock. L : Lock
37	MCK2	I/O	FS converter section master clock input/output pin
38	IOSEL	I	MCK2 I/O selection signal input pin. H : Output. L : Input
39	AVDD	–	Analog power supply pin
40	MUTE	I	Mute control signal input pin. H : Soft mute. L : Off

Pin No.	Name	I/O	Function
41	FSEL3	I	Output data fs selection signal input pin. H : 2 fs. L : fs
42	TEST	I	For test
43	DVDD	–	Ground pin
44	DLSEL	I	Digital filter output bit number setting input pin. H : 20 bits. L : 18 bits
45	FSEL2	I	Input fs selection input pin 2. H : 32 kHz. L : 48 kHz
46	FSEL1	I	Input fs selection input pin 1. H : 48 or 32 kHz. L : 44.1 khz
47	MSEL2	I	Operation mode selection input pin 2. H : Single FSC mode. L : Single DF mode
48	MSEL1	I	Operation mode selection input pin 1. H : Single operations. L : Normal operations

■ PDC019A (AUDIO DIGITAL BOARD ASSY, IC301) EFM ENCODER

● Block Diagram


DIRLPF,DIRVCO,
DIRRC1,DIRRC2,
DIRRS,DIRERR
DIRU,
DIRWDCK
DIRDATA,
DIRBCK,
DIRLRCK,DIRCK
CDTX
DIN1-4
DIR
DIT
DITOUT
CDDATA,
CDBCK,
CDLRCK
DATSEL
FADER
LEVEL METER
MUTE
DACDATA,
DACBCK,
DACLRCK
ADCDATA
ADCSTBY
ADCCLK,
ADCBCK,
ADCLRCK
MEMCON
A9-0,DQ4-1,
RAS,CAS,
OE,WR
CLKSEL
DACCKOUT
ENCCKOUT
JITVCOIN
CJSDATA,
CJSBCK,
CJSLRCK
CJS
CLKGEN
PLL
ENCPCO,
ENCLPFI,
ENCLPFO,
ENCERR
JITPCO,
JITLPFI,
JITLPFO,
JITERR
RAM
CDENC
ENCVCOIN,
ENCCK,
RFDET,
RECEN,
EXTSYNC,
EXTACK,
ATIPSYNC,
SUBSYNC
XTALIN
XTALOUT
SUBCODE
RESET
MICON I/F
STRATEGY
EFM,
DEC3T,DECIT
XSAMPLE
DRAMSW
CCB,
CE,CL,DI,DO

● Pin Function

Pin No.	Name	I/O	Function
1	DIN 1	I	Optical module responding data input pin
2	DIN 2	I	Optical module responding data input pin
3	DIN 3	I	Optical module responding data input pin
4	DIN 4	I	Optical module responding data input pin
5	DIRRC 1	I	RC oscillation input pin
6	DIRRC 2	O	RC oscillation output pin
7	AVDD	–	Analog power supply pin
8	DIRRS	I	VCO oscillation band adjustment input pin
9	AGND	–	Analog ground pin
10	DIRVCO	I	VCO freerunning oscillation setting input pin
11	DIRLPF	O	PLL low pass filter pin
12	VSS	–	Ground pin
13	VDD	–	+5V power supply pin
14	DIRCK	O	DIR system clock output pin
15	DIRBCK	O	DIR bit clock output pin
16	DIRLRCK	O	DIR LR clock output pin
17	DIRDATA	O	DIR demodulation data output pin
18	DIRWDCK	O	DIR word clock output pin
19	DIRU	O	User bit output pin
20	DIRERR	O	Data error or lock state monitor output pin. H : Unlocked. L : Locked
21	DRAMSW	O	External DRAM capacity setting output pin. H : 4Mbit. L : 1Mbit
22	CJSDATA	I	Clock jitter suppresser data input pin
23	CJSBCK	I	Clock jitter suppresser bit clock input pin
24	CJSLRCK	I	Clock jitter suppresser LR clock input pin
25	JITVCOIN	I	VCO input pin
26	JITLPFO	O	LPF output pin
27	JITLPFI	I	LPF input pin
28	JITPCO	O	Phase comparator output pin
29	JITERR	O	Lock state monitor signal output pin. H : Unlocked. L : Locked
30	DACDATA	O	DAC data output pin
31	DACBCK	O	DAC bit clock output pin
32	DACLRCK	O	DAC LR clock output pin
33	ADCDATA	I	ADC recording data input pin
34	ADCCLK	O	ADC clock output pin
35	ADCBCK	O	ADC bit clock output pin
36	ADCLRCK	O	ADC LR clock output pin
37	ADCSTBY	O	ADC standby signal output pin. H:Operating. L:Standby
38	XTALIN	I	System clock input pin
39	XTALOUT	O	System clock output pin
40	VSS	–	Ground pin

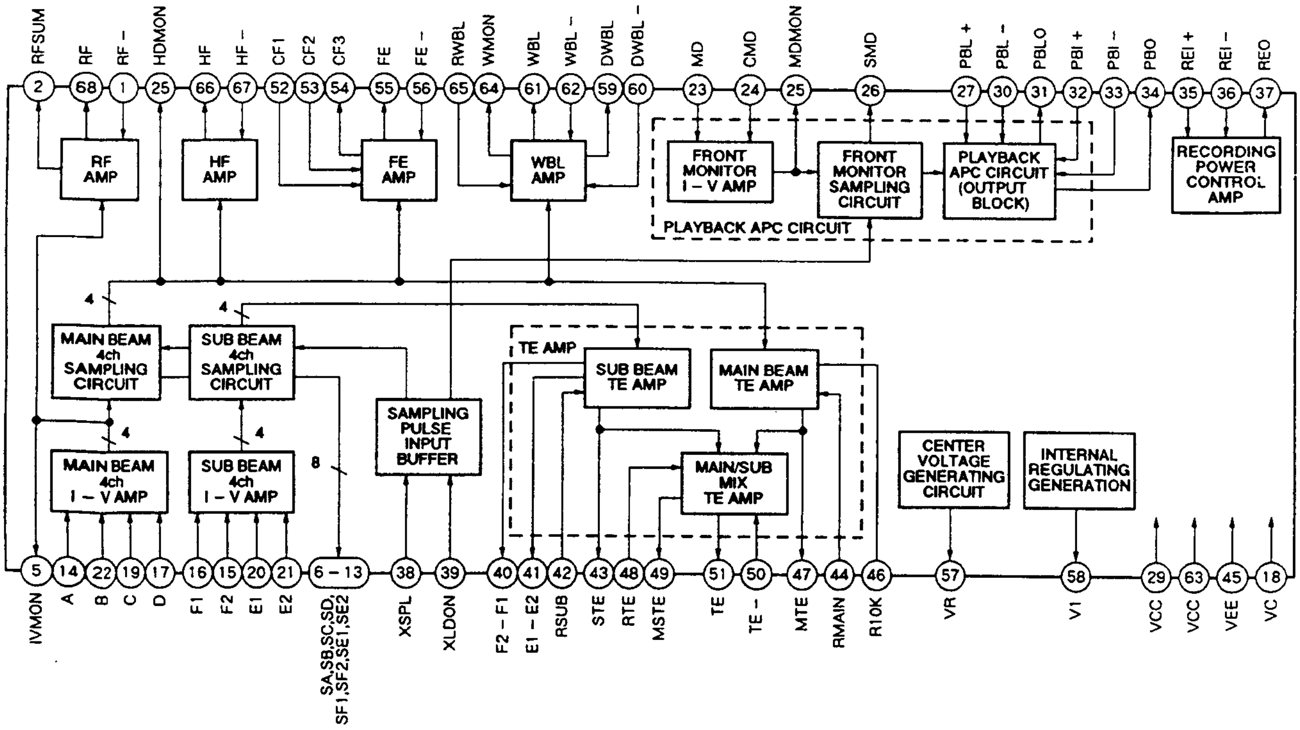
Pin No.	Name	I/O	Function
41	VDD	–	+5V power supply pin
42	DACCKOUT	O	DAC system clock output pin
43	ENCCKOUT	O	CD decoder system clock output pin
44	CDDATA	I	CD decoder data input pin
45	CDBCK	I	CD decoder bit clock input pin
46	CDLRCK	I	CD decoder LR clock input pin
47	CDTX	I	Pin for inputting signal from CD decoder output
48	DITOUT	O	Bi-phase modulation output pin
49	TP6	I	For tests
50	XRESET	I	System reset input pin. L : Reset
51	TP7	I	For tests
52	XCAS	O	DRAM row address strobe signal output pin
53	XOE	O	DRAM output enable signal output pin
54	A8	O	DRAM address output pin
55	A7	O	
56	A6	O	
57	A5	O	
58	A4	O	
59	A3	O	
60	A2	O	
61	VDD	–	+5V power supply pin
62	VSS	–	Ground pin
63	A1	O	DRAM address output pin
64	A0	O	
65	A9	O	
66	XRAS	O	DRAM column address strobe signal output pin
67	XWR	O	DRAM read/write signal output pin
68	DQ2	I/O	DRAM data input/output pin
69	DQ1	I/O	
70	DQ4	I/O	
71	DQ3	I/O	
72	TP0	I	For tests
73	TP1	I	
74	TP2	I	
75	TP3	O	
76	ENCVCOIN	I	Encode circuit clock input pin
77	ENCLPFO	O	LPF output pin
78	ENCLPFI	I	LPF input pin
79	ENCPCO	O	Phase comparator output pin
80	ENCERR	O	Lock state monitor signal output pin. H : Unlocked. L : Locked

Pin No.	Name	I/O	Function
81	TP4	O	For tests
82	TP5	I	
83	XRFDET	I	RF detection signal input pin. H : No RF. L : RF
84	RECEN	I	Recording enable signal input pin. H : Recordable. L : Not recordable
85	XSAMPLE	O	Sample pulse signal for sample servo output pin
86	DET4T	O	4T detection signal output pin
87	DET3T	O	3T detection signal output pin
88	EFM	O	EFM signal output pin
89	VDD	–	+5V power supply pin
90	VSS	–	Ground pin
91	ENCCK	O	Encode clock output pin
92	XEXTACK	O	ATIP synchronization notification signal output pin
93	XEXTSYNC	I	ATIP synchronization enable signal input pin
94	ATIPSYNC	I	ATIP sync signal input pin
95	SUBSYNC	O	Subcode sync signal output pin
96	CCB	I	CPU interface method selection signal input pin. H : Sanyo CCB format. L : General serial format
97	CE	I	CPU interface chip enable signal input pin
98	CL	I	CPU interface data transfer clock input pin
99	DI	I	CPU interface data input pin
100	DO	O	CPU interface data output pin

■ PA4022A (HEAD BOARD ASSY, IC101)

RF Amplifier

● Block Diagram


RFSUM ②
RF (68)
RF – ①
HDMON (25)
HF (66)
HF – (67)
CF1 (52)
CF2 (53)
CF3 (54)
FE (55)
FE – (56)
RWBL (65)
WMON (64)
WBL (61)
WBL – (62)
DWBL (59)
DWBL – (60)
MD (23)
CMD (24)
MDMON (25)
SMD (26)
PBL + (27)
PBL – (30)
PBLO (31)
PBI + (32)
PBI – (33)
PBO (34)
REI + (35)
REI – (36)
REO (37)
RF AMP
HF AMP
FE AMP
WBL AMP
FRONT MONITOR I – V AMP
FRONT MONITOR SAMPLING CIRCUIT
PLAYBACK APC CIRCUIT (OUTPUT BLOCK)
PLAYBACK APC CIRCUIT
RECORDING POWER CONTROL AMP
4
4
MAIN BEAM 4ch SAMPLING CIRCUIT
SUB BEAM 4ch SAMPLING CIRCUIT
4
4
MAIN BEAM 4ch I – V AMP
SUB BEAM 4ch I – V AMP
8
SAMPLING PULSE INPUT BUFFER
TE AMP
SUB BEAM TE AMP
MAIN BEAM TE AMP
MAIN/SUB MIX TE AMP
CENTER VOLTAGE GENERATING CIRCUIT
INTERNAL REGULATING GENERATION
⑤ IVMON
⑭ A
(22) B
⑲ C
⑰ D
⑯ F1
⑮ F2
⑳ E1
(21) E2
6 – 13 SA,SB,SC,SD, SF1,SF2,SE1,SE2
(38) XSPL
(39) XLDON
(40) F2 – F1
(41) E1 – E2
(42) RSUB
(43) STE
(48) RTE
(49) MSTE
(51) TE
(50) TE –
(47) MTE
(44) RMAIN
(46) R10K
(57) VR
(58) V1
(29) VCC
(63) VCC
(45) VEE
⑱ VC

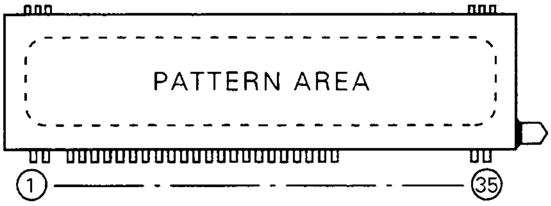
- **Pin Function**

Pin No.	Name	I/O	Function
1	RF–	I	RF amplifier inversion input pin
2	RFSUM	O	RF summing amplifier output pin
3	HDMON	O	Sample hold signal monitor output pin
4	VEE	–	-5V power supply pin
5	IVMON	O	I-V amplifier output monitor pin
6	SA	O	Sample hold capacitor connection pin
7	SB	O	
8	SC	O	
9	SD	O	
10	SF1	O	
11	SF2	O	
12	SE1	O	
13	SE2	O	
14	A	I	Detector current input pin
15	F2	I	
16	F1	I	
17	D	I	
18	VC	I	Middle point voltage (GND) connection pin
19	C	I	Detector current input pin
20	E1	I	
21	E2	I	
22	B	I	
23	MD	I	Monitor diode current input pin
24	CMD	I	Playback laser APC I-V amplifier non-inversion input pin
25	MDMON	O	Playback laser APC I-V amplifier output pin
26	SMD	O	Playback laser APC hold output
27	PBL+	I	Playback laser APC loop gain setting amplifier non-inversion input pin
28	N. C.	-	Not used
29	VCC	–	+5V power supply pin
30	PBL–	I	Playback laser APC loop gain setting amplifier inversion input pin
31	PBLO	O	Playback laser APC loop gain setting amplifier output pin
32	PBI+	I	Playback laser APC voltage current conversion amplifier non-inversion input pin
33	PBI–	I	Playback laser APC voltage current conversion amplifier inversion input pin
34	PBO	O	Playback laser APC voltage current conversion output pin
35	REI+	I	Recording laser power current setting amplifier non-inversion input pin
36	REI–	I	Recording laser power current setting amplifier inversion input pin
37	REO	O	Recording laser power current setting amplifier output amplifier
38	XSPL	I	Sample pulse input pin. H : Hold. L : Sampling
39	XLDON	I	Laser diode ON/OFF control signal input pin. H : OFF. L : ON
40	F2–F1	O	Subbeam F push-pull signal monitor output pin

Pin No.	Name	I/O	Function
41	E1–E2	O	Subbeam E push-pull signal monitor output pin
42	RSUB	I	Subbeam gain difference adjustment control connection pin
43	STE	O	Subbeam differential amplifier output pin
44	RMAIN	I	Main beam tracking balance adjustment control connection pin
45	VEE	-	-5V connection pin
46	R10K	-	Internal 10 kΩ resistor
47	MTE	O	Main beam differential amplifier output pin
48	RTE	O	Main/sub gain differential adjustment control connection pin
49	MSTE	O	DPP signal output pin
50	TE–	I	Tracking error level adjustment amplifier inversion input pin
51	TE	O	Tracking error level adjustment amplifier output pin
52	CF1	I	Focus error band limitation capacity connection pin
53	CF2	I	Focus error band limitation capacity connection pin
54	CF3	O	Focus error band limitation capacity connection pin
55	FE	O	Focus error level adjustment amplifier output pin
56	FE–	I	Focus error level adjustment amplifier inversion input pin
57	VR	O	Middle point potential generation circuit output pin
58	V1	O	Internal power supply monitor output pin
59	DWBL	O	WOBBLE balance circuit LPF amplifier output pin
60	DWBL–	I	WOBBLE balance circuit LPF amplifier inversion input pin
61	WBL	O	WOBBLE signal generation amplifier output pin
62	WBL–	I	WOBBLE signal generation amplifier inversion input pin
63	VCC	–	+5V input pin
64	WMON	O	WOBBLE push-pull signal monitor output pin
65	RWBL	I	WOBBLE balance circuit variable resistor connection pin
66	HF	O	HF signal output pin
67	HF–	I	HF amplifier inversion input pin
68	RF	O	RF signal output pin

10. FL INFORMATION

■ PEL1086 (V701: FUNCTION BOARD ASSY)


PATTERN AREA
①
㉟

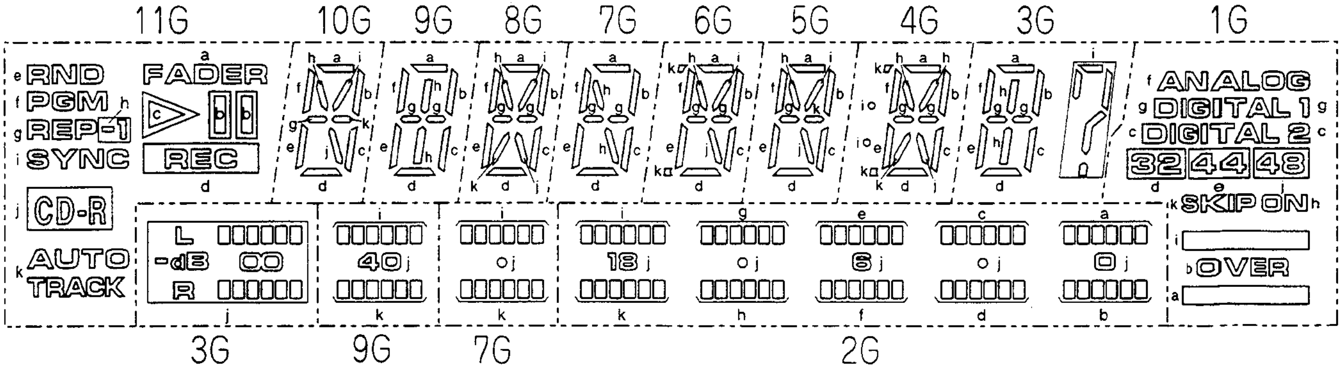
Pin Connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Connection	F1	F1	NP	P_a	P_b	P_c	P_d	P_e	P_f	P_g	P_h	P_i	P_j	P_k	11G	10G	9G

Pin No.	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
Connection	8G	7G	6G	5G	4G	3G	2G	1G	NP	NP	NP	NP	NP	NP	NP	NP	F2	F2

Notes : 1) F: Filament 2) G: Grid 3) P: Anode 4) NP : No Pin

Grid Assignment


11G
10G
9G
8G
7G
6G
5G
4G
3G
1G
RND
PGM
REP-1
SYNC
FADER
REC
CD-R
AUTO TRACK
L
-dB
R
40
18
6
0
ANALOG
DIGITAL 1
DIGITAL 2
32
44
48
SKIP
ON
OVER
3G
9G
7G
2G

Anode Connection

	11G	10G	9G	8G	7G	6G	5G	4G	3G	2G	1G
a	FADER	a	a	a	a	a	a	a	a	a	▭
b	▯▯	b	b	b	b	b	b	b	b	b	OVER
c	▷	c	c	c	c	c	c	c	c	c	DIGITAL 2
d	REC	d	d	d	d	d	d	d	d	d	32
e	RND	e	e	e	e	e	e	e	e	e	44
f	PGM	f	f	f	f	f	f	f	f	f	ANALOG
g	REP	g	g	g	g	g	g	g	g	g	DIGITAL 1
h	-1	h	h	h	h	h	h	h	h	h	ON
i	SYNC	i	i	i	i	i	i	i	i	i	▭
j	CD-R	j	j	j	j	j	j	j	j	j	48
k	AUTO TRACK		k	k	k	k	k	k		k	SKIP

11. CIRCUIT DESCRIPTION

11.1 CD-R DISC

As shown in Fig. 11-1, the CD-R disc is composed of first a recording layer, then a reflection layer, and then a protection layer (these are all color pigment layers) on top of a resin board. Guiding grooves called grooves are opened on the disc. By irradiating strong laser power on these grooves during recording, the color pigments change and pits are formed. The grooves have certain frequency undulations called wobble. The speed of the disc is controlled according to these wobbles. These wobbles are FM-modulated, enabling information on the absolute time, etc. of the disc to be obtained.

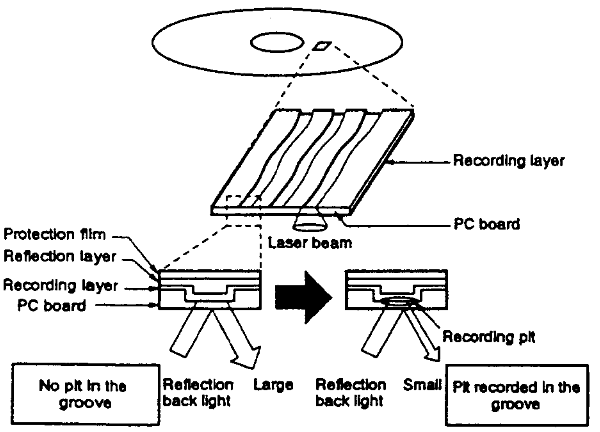

Recording layer
PC board
Protection film
Reflection layer
Recording layer
PC board
Laser beam
Recording pit
No pit in the groove
Reflection back light
Large
Reflection back light
Small
Pit recorded in the groove

Fig. 11-1 CD-R disc structure

11.2 PICKUP

11.2.1 Optical Path of Pickup

Fig. 11-2 shows the internal structure of the pickup. This pickup for recording differs from the normal CD pickup in that, to increase the power generated from the objective lens, the optical system is unlimited, and the laser diode is high output.

If the flow of light is explained based on the optical diagram, first the distributed light from the laser diode is converted to parallel light by the collimator lens, divided into three beams by grating, and directed towards the beam splitter. The light from the laser diode is oval-shaped, and it is made round by the refraction at the plane of incidence of the beam splitter. Some of the light at this time is reflected and induced by the monitor photo diode and used for controlling the power of the laser diode. The light output from the shaping beam splitter is passed through the reflection prism and wave length board, and converged at three spots on the disc by the objective lens.

The light reflected on the disc again is passed through the objective lens and becomes parallel light again, is passed through the reflection prism and shaping beam splitter, and moves towards the convex lens. After non-point aberration is generated by the multi lens, it enters the 8-divided photo diode. The information signal and focus signal of the disc are formed by the 4 divided parts at the center of the photo diode, and the tracking signal is made by synthesizing all the parts described below.

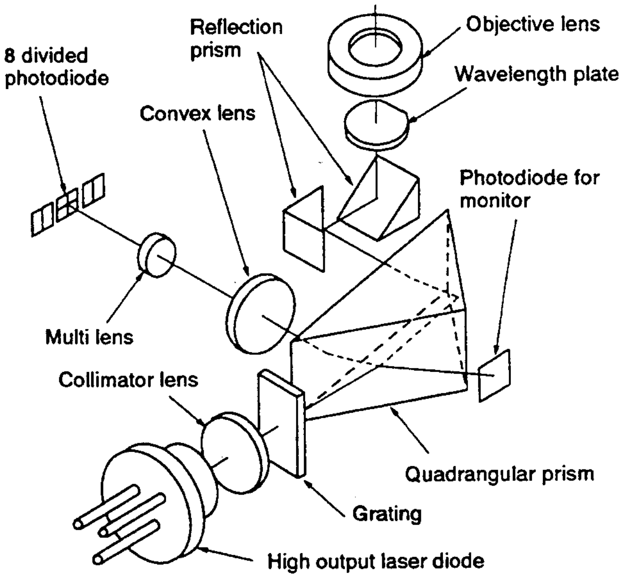
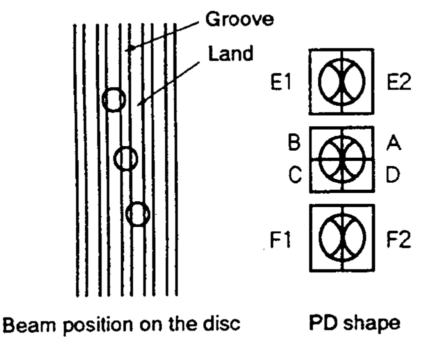

Reflection prism
Objective lens
8 divided photodiode
Wavelength plate
Convex lens
Photodiode for monitor
Multi lens
Collimator lens
Quadrangular prism
Grating
High output laser diode

Fig. 11-2 Structure of pickup

11.2.2 Servo Method

The focus servo adopts the non-point aberration method like normal CDs. The 3-beam method, like normal CDs, cannot be used for the tracking servo. This is because the 3-beam method senses the brightness/darkness of the disc and servo cannot be imposed in all bright states of the disc before recording. For this reason, the push-pull method is adopted, in which the diffraction light generated by the grooves on the disc are used. By obtaining the right and left difference of the light returning to the photo diode, the tracking signal is obtained. However, with one push-pull signal, offset is generated due to the changes caused by the objective lens following the disc, or the offset generated due to the distortion of the disc. Therefore, as shown in Fig. 11-3, this unit uses the differential push-pull method in which offset is canceled by synthesizing the push-pull signals of the three beams.


Groove
Land
E1
E2
B
A
C
D
F1
F2
Beam position on the disc
PD shape

$$TE = [(A + D) - (B + C)] - \frac{K}{2}[(E2 - E1) + (F2 - F1)]$$

(K=0 – primary light ratio)

Fig. 11-3 Tracking system

11.3 Servo Section

11.3.1 APC

In this unit laser power control for playback and recording differs. During playback, APC (auto power control) similar to the CD player is basically performed, and during recording, control unique to the CD-R is performed.

During playback, the power output from the laser diode of the pickup is detected by the monitor diode and the detected signal is input from the MD (Pin 23) of the RF amplifier IC (IC101 : PA4022A). After current-voltage (I/V) conversion, it is amplified. Next, the output compared with the voltage of VR103 determining the playback power is input to the voltage-current (V/I) conversion circuit composed of the internal ope-amplifier of the IC and Q102 and applied to the laser diode. In this way, as the circuit operates so that the current detected by the monitor diode becomes constant, the laser power is always constant regardless of changes in temperature etc.

During recording, the APC for playback also functions. Only when pit is generated is the laser power required for recording generated. To ensure that no level changes occur in the servo signal during recording, the APC functions in the sample hold circuit of the RF amplifier IC using a signal generated by laser power not used for generating pits.

As the recording power changes according to the inconsistency of the disc, it is necessary to control the power to the optimum value each time (OPC adjustment). This value is converted to DC. voltage value by the DA converter inside the CDR servo amplifier IC (IC205 : PA9004A) according to the data passing through the ATIP decoder IC (IC207 : PDJ006A) from the mechanism control microprocessor (ICC356 : PD4584A, hereafter referred to mechanism controller) of the servo microprocessor board assembly. It is then input to the ope-amplifier in the RF amplifier IC and the V/I conversion circuit of Q101. This current is current-amplified by the mirror circuit composed of Q103 to Q106, and supplied to the laser diode by the Q107 collector. This current is turned on/off by IC103 and Q108 according to the recording signal from the EFM encoder IC (IC301 : PDC019A) to form the pit rows in the disc.

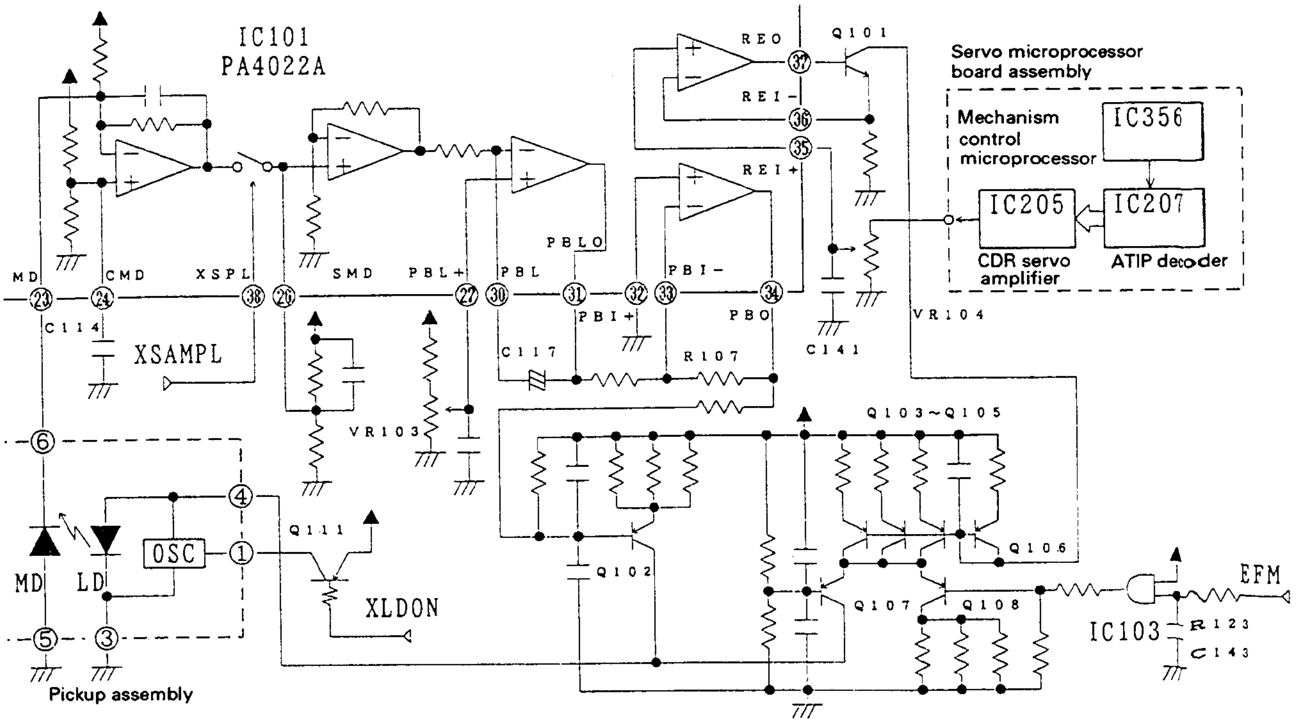

IC101
PA4022A
REO
Q101
REI −
REI +
Servo microprocessor board assembly
Mechanism control microprocessor
IC356
IC205
IC207
CDR servo amplifier
ATIP decoder
PBLO
MD
CMD
XSPL
SMD
PBL+
PBL
PBI −
PBI +
PBO
㉓
㉔
㊳
㉖
㉗
㉚
㉛
㉜
㉝
㉞
㉟
㊱
㊲
C114
XSAMPL
C117
R107
C141
VR104
VR103
Q103~Q105
Q106
Q107
Q108
Q102
Q111
XLDON
⑥
④
①
⑤
③
OSC
MD
LD
EFM
IC103
R123
C143
Pickup assembly

Fig. 11-4 APC peripheral circuit

11.3.2 Error Signal Generation Circuit

As the 3-beam differential push-pull method is used for the pickup of this unit, a pickup main beam 4-divided detector and two sub-beam 2-divided detector are provided. The current output is I-V converted respectively as shown in Fig. 11-5 for generating the HF, RF, wobble, focus error, and tracking error.

The outputs A, B, C, D, E1, E2, F1, and F2 of the detector are input to Pins 14, 22, 19, 17, 20, 21, 16, and 15 of the RF amplifier IC. After I-V conversion, it is led to the sample hold circuit. This sample hold circuit is provided so that each error signals for recording can be generated consistently. It is controlled so that it samples outputs when no pit is generated and holds outputs when pits are generated (when the laser generates recording power).

After the outputs of the sample hold circuit are amplified, the HF, RF, focus error are generated in a manner that the main beam output is calculated in the same way as the CD player, and then output to Pins 66, 68, and 55 respectively.

As shown in Fig. 11-6, the focus error is offset-adjusted by VR105 connected to Pin 56, and offset variations caused by temperature changes are canceled by the R148 temperature compensation resistance. Furthermore, when ATIP signals are required for the CD-R disc, focus error is separately adjusted by the circuit composed of Q115 to 117, and VR115 for more reliable performance.

As shown in Fig. 11-7, the tracking error is created by generating the main beam push-pull signal and sub beam push-pull signal, and adding/subtracting these. The light amount balance of the main beam and subbeam is adjusted at VR110 connected to Pin 48 and then output to Pin 49. This output is further gain-adjusted by VR111, offset-adjusted by VR112, input to the RF amplifier IC from Pin 50, amplified and finally output to Pin 51 as the following signal.

$$[(A + D) - (B + C)] - K [(E2 - E1) + (F2 - F1)] / 2$$

(K = 0-1 stage light amount ratio)

Fig. 11-8 shows the wobble generation circuit. The wobble signal is generated by the main beam so that the calculation [(A+D)-(B+C)] is performed and output from Pin 61. To prevent C/N deterioration due to the lost in balance of the left and right sides due to the deviation of the disc eccentricity and optical axis of the beam which disables the cancellation of RF components, etc., the auto balance circuit provides good wobble signals at all times.

This circuit passes the calculated output mentioned earlier through the inverting amplifier band-limited to the maximum frequency of eccentricity, and the output is fed back to the FET (Q110) connected to the calculation circuit of the first stage. The FET operates as a variable resistance element.

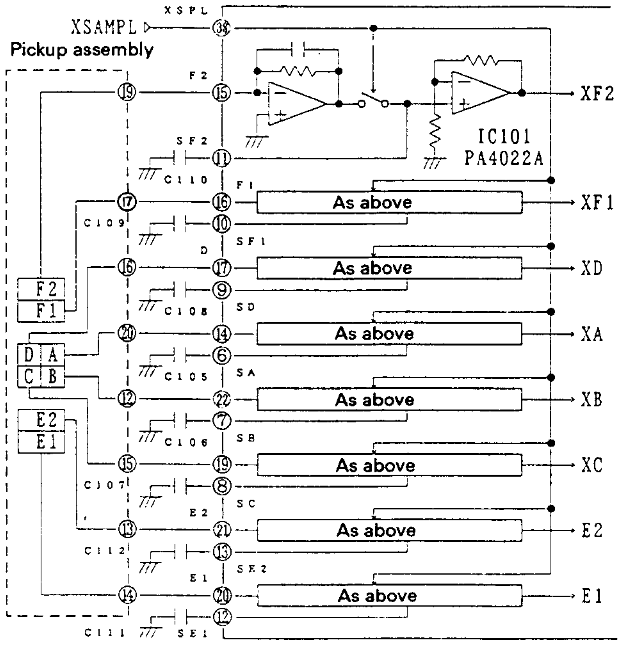
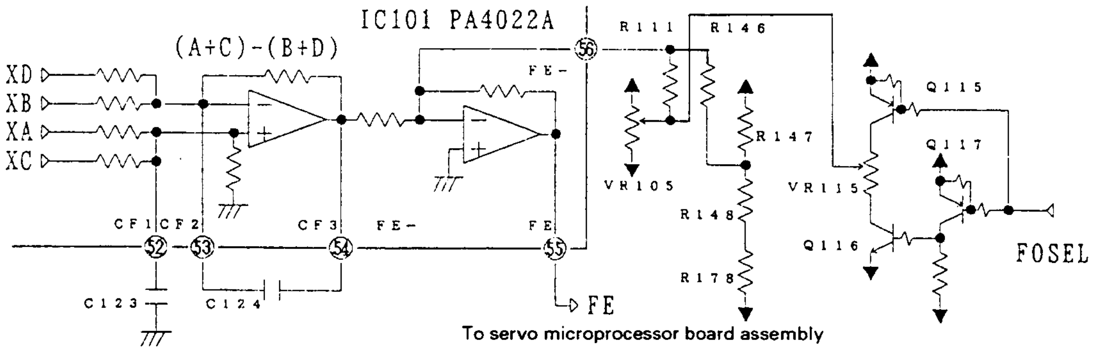


Fig. 11-5 I/V conversion circuit



To servo microprocessor board assembly

Fig. 11-6 Focus error generation circuit

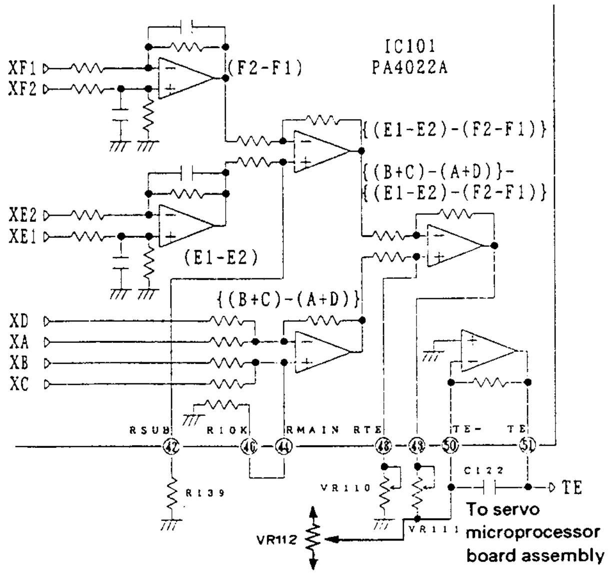

IC101
PA4022A
XF1
XF2
(F2-F1)
{(E1-E2)-(F2-F1)}
{(B+C)-(A+D)}-
{(E1-E2)-(F2-F1)}
XE2
XE1
(E1-E2)
{(B+C)-(A+D)}
XD
XA
XB
XC
RSUB
RIOK
RMAIN
RTE
TE-
TE
42
46
44
43
49
50
51
R139
VR110
C122
TE
To servo microprocessor board assembly
VR111
VR112

Fig. 11-7 Tracking error generation circuit

11.3.3 Sample Hold Pulse Generation Circuit

During recording, only during pit generation is the laser power set to the recordable level. Consequently, the level of the light reflected from the disc differs during pit generation and playback level and thus disables normal servo errors from being obtained. This unit therefore uses a sample hold method for extracting signals only during playback.

The sample pulse is a signal which remains level L about 500 nsec after the falling of the recording EFM signal to its rising. This pulse is output from the EFM encoder IC and input to Pin 38 of the RF amplifier IC as XSAMPL.

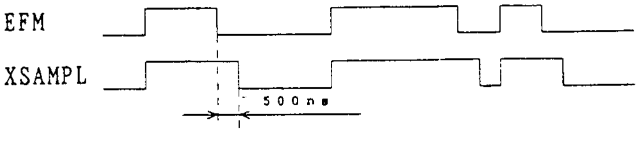


Fig. 11-9 Sample hold pulse timing

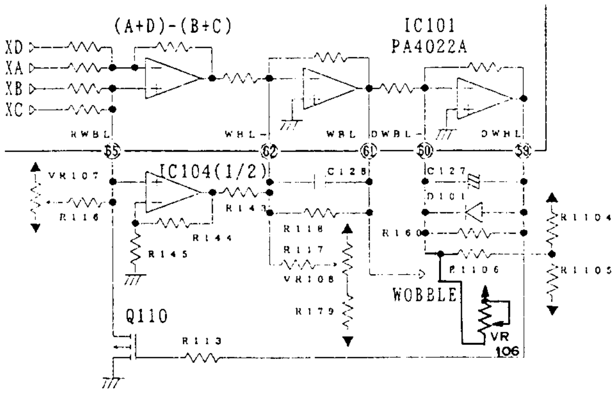

(A+D)-(B+C)
IC101
PA4022A
XD
XA
XB
XC
RWBL
WHL
WBL
DWBL
DWHL
55
62
61
60
58
VR107
IC104(1/2)
R116
C128
C127
D101
R147
R144
R145
R118
R117
VR108
R160
R1106
R1104
R1105
WOBBLE
VR 106
Q110
R179
R113

Fig. 11-8 Wobble generation circuit

11.3.4 Focus Servo

As shown in Fig. 11-10, the focus servo system of this unit is the same as the CD player. The error signal generated in the RF amplifier IC is led to the servo microprocessor board assembly via CN105, adjusted for its loop gain in VR201, and input to FE (Pin 47) and FZC (Pin 46) of the servo control IC for CD (IC201 : CXA1372Q). It is then passed through the defect countermeasure circuit and phase compensation circuit inside the IC and output from FEO (Pin 5). This output is led to the head board assembly and supplied to the focus actuator drive coil by the power ope-amplifier (IC202 : LA6517).

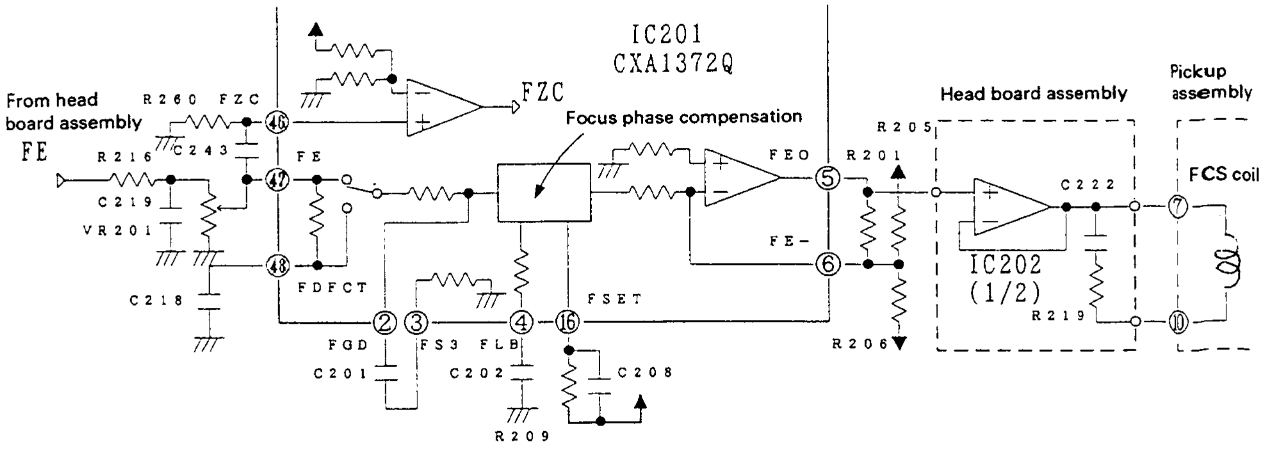

IC201
CXA1372Q
From head board assembly
R260
FZC
FE
R216
C243
C219
VR201
C218
46
47
48
FZC
Focus phase compensation
FE
FDFCT
FEO
FE-
FGD
FS3
FLB
FSET
C201
C202
C208
R209
2
3
4
16
5
6
R205
R201
R206
Head board assembly
C222
IC202
(1/2)
R219
Pickup assembly
FCS coil
7
10

Fig. 11-10 Focus servo circuit

11.3.5 Tracking Sled Servo

Fig. 11-11 shows the tracking sled servo system of this unit. The error signals generated in this RF amplifier IC is led to the servo microprocessor board assembly via CN105 and input to TE (Pin 29) of the CD-R servo amplifier IC. This variable gain amplifier is provided to control gain inconsistency of the tracking error signal of each disc, and set the optimum loop characteristics. First, the tracking servo is set to open when TEG0 to TEG2, and TEGM are in a certain condition. The mechanism controller then measures the TEDET (Pin 36) level. From the results, the combination of TEG0 to 2 and TEGM are calculated to set the optimum level of the mechanism controller and reset. The TEDET is a result of detection of the P-P value of the signal passing through the variable gain amplifier and converted to DC. voltage by the external resistor and capacitor.

The output from TRKGR (Pin 32) is passed through the VR202 for loop gain adjustment and input to TE (Pin 43) of the servo control IC for CD. It is then passed through the defect countermeasure circuit and phase compensation circuit inside the IC and is output from TAO (Pin 11). This output is then led to the head board assembly after passing through the switch for selecting the actuator hold amplifier (IC5008 (1/2)) output and supplied to the tracking actuator drive coil by the power ope-amplifier (IC202 : LA6517).

Immediately after jumping, the actuator hold is switched from the normal tracking servo loop by the mechanism controller during especially long distance jumps to reduce the time taken for adjusting the actuator and preventing the closing of the tracking servo loop in the incorrect state. This prevents unwanted operations of the actuator and enables accurate address information to be obtained in a short time after jumps.

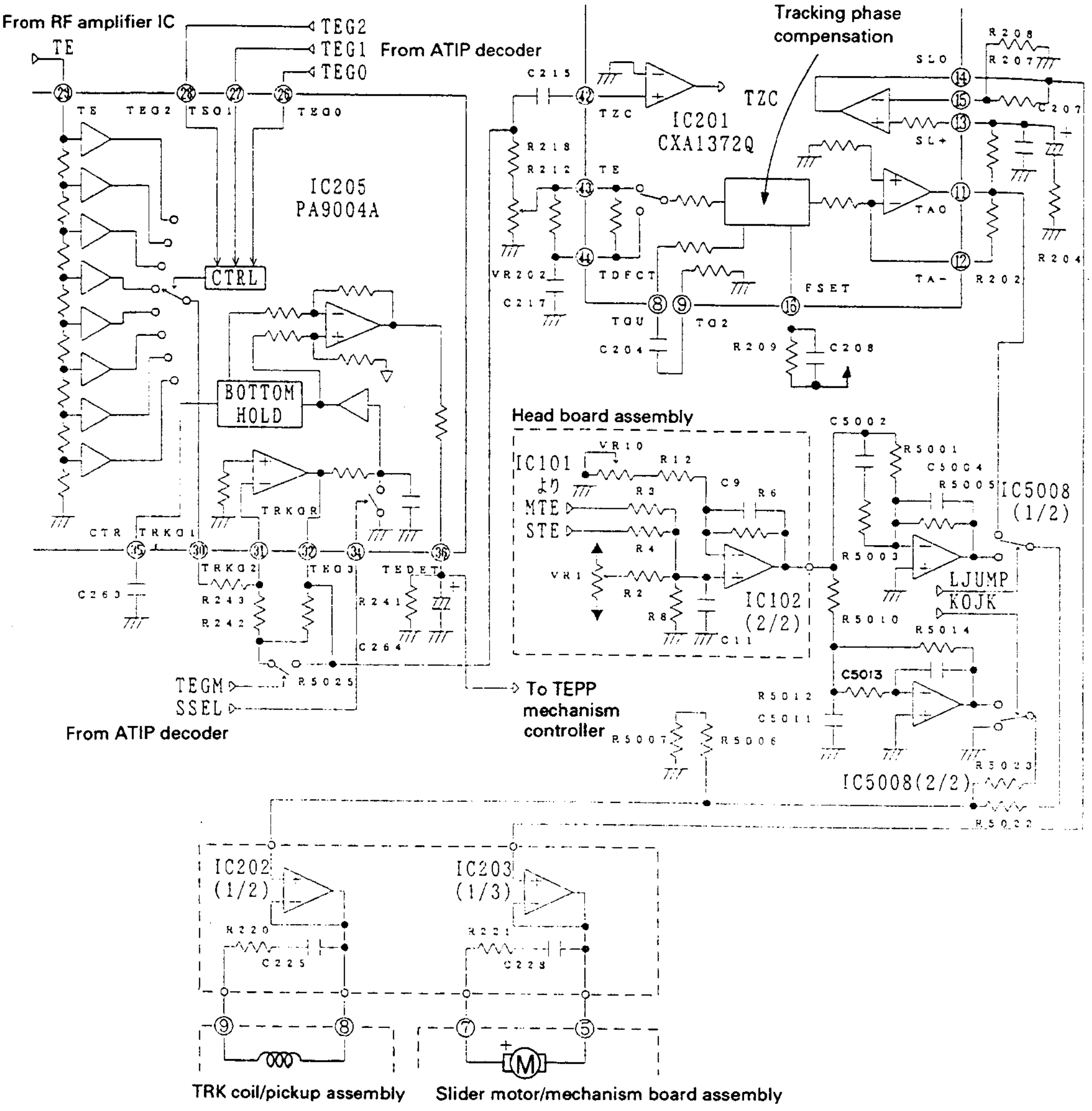

From RF amplifier IC
TE
TEG2
TEG1
TEG0
From ATIP decoder
IC205
PA9004A
CTRL
BOTTOM HOLD
TRKGR
CTR
TRKG1
TRKG2
TEG3
TEDET
R243
R242
R241
C263
C264
TEGM
SSEL
R5025
From ATIP decoder
To TEPP mechanism controller
C215
R218
R212
VR202
C217
TZC
TE
IC201
CXA1372Q
TZC
TDFCT
TOU
TO2
C204
R209
C208
FSET
Tracking phase compensation
SLO
SL+
TAO
TA-
R208
R207
R204
R202
Head board assembly
IC101
VR10
R12
R3
C9
R6
MTE
STE
R4
VR1
R2
R8
IC102 (2/2)
C11
C5002
R5001
C5004
R5005
IC5008 (1/2)
R5003
LJUMP
KOJK
R5010
R5014
C5013
R5012
C5011
R5007
R5006
IC5008(2/2)
R5023
R5022
IC202 (1/2)
IC203 (1/3)
R220
C225
R221
C223
M
TRK coil/pickup assembly
Slider motor/mechanism board assembly

Fig. 11-11 Tracking servo circuit

In order to read wobble signals of CD-R disc more accurately, this unit adopts the optical axis servo. This servo only functions during the playback of CD-R discs and prevents the degradation of read signal due to the incorrect position of optical axis of the pickup during playing back.

The output of the optical axis servo amplifier (IC5008 (2/2)) is added to the control signal of the tracking actuator, including the normal tracking servo loop, and operates as double loop.

The signal used for actuator hold and optical axis servo is extracted from the main beam push-pull signal output from MTE (Pin 47) of the RF amplifier IC and subbeam push-pull signal output from STE (Pin 43). In this case a method is oppositely used in which, for normal tracking error signals, the cancellation of the DC offset components is executed by the differential push-pull method.

The TAO output, on the other hand, is passed through the low pass filter (LPF) and input to SL+(Pin 13) of the servo control IC for CDs. So, this is also a input of the sled servo system, like CD players. The slider control signal output from SLO (Pin 14) is led to the head board assembly via CN106 and supplied to the slider motor by the driver IC (IC203 (1/3)).

11.3.6 Spindle Servo

Fig. 11-12 shows the block diagram, of the spindle servo. Different types of spindle control is performed in this unit during playback of recorded parts, playback and recording of unrecorded parts, and change of number of rotations.

First, the playback of recorded parts is the same as CD players. RF signals generated in the RF amplifier IC is passed through CN105, is led to the servo microprocessor board assembly, and input to the RFI (Pin 39) of the servo control IC for CDs. The RF signal input is converted to a binary signal by the comparator, output to EFM (Pin 32), and input to the RF (Pin 24) of the CD decoder IC (IC206 : CXD2500BQ). MDP errors are generated from the sync signal in the EFM signal and the internal reference signal. In this IC, processes hereafter are performed digitally, and finally, ternary PWM signals are output to MDP (Pin 4), input as PWM 3 to the CDR servo amplifier IC, and becomes the spindle control signal whose carrier components have been eliminated by the filter.

As the above mentioned sync signal does not exist during the playback and recording of unrecorded parts, the rotation control signal of the disc called wobbles are read from the grooves on the disc beforehand. Information on the absolute time called ATIP are also obtained from these signals.

In the normal operations of this unit, the rotation of the spindle motor is brought near the rotation speed at the targeted location of the disc by CAV control (angular velocity is constant) which uses the PWM output of the mechanism controller, and then spindle servo using wobbles is selected. In this wobble servo, first the wobble signal generated in the RF amplifier IC is passed through the band pass filter (BPF) of IC104 (2/2), passed through CN105, is led to the servo microprocessor board assembly, eliminated for unnecessary components by the 22.05 kHz BPF composed of Pins 38 to 43 of the CDR servo amplifier IC, binarized by the comparator, and output to WBLO (Pin 45). This signal is then input to WBL (Pin 1) of the ATIP decoder IC. In this IC, the 4.3218 MHz supplied from the EFM encoder IC serves as the master clock. By comparing the phase with the earlier mentioned wobble signal based on the frequency division of this master clock (22.05 kHz), the binary PWM signal is output. This output is input as PWM2 to the CDR servo amplifier IC. At the same time carrier components are eliminated by the filter, phase compensation and gain compensation are performed so that it becomes the spindle control signal.

Apart from the wobble servo, this ATIP decoder also demodulates information such as ATIP sync, absolute time, recommended recording power, lead-in area starting time, read-out area starting time, and disc application from the wobble signal, and sends them to the mechanism controller.

When the rotation speed of the spindle motor is changed rapidly during start, stop, search, etc., it is switched to CAV by the mechanism controller. As the current rotation speed information can be obtained because the mechanism controller counts the FG signal obtained from the servo mechanism, it can be changed to the desired rotation speed in a short time. The PWM output from the mechanism controller is input to the CDR servo amplifier IC as PWM1.

The above three spindle control signals are switched inside the CDR servo amplifier IC according to the operation mode, output from SPDLO (Pin 9), and the rotation of the spindle motor is controlled by the spindle driver IC (IC203 : LA6520) of the head board assembly.

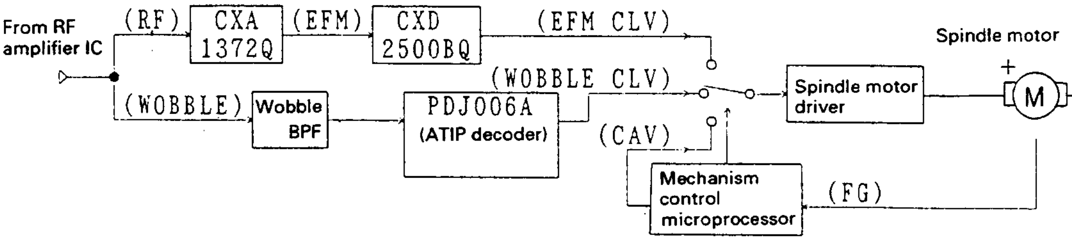


Fig. 11-12 Spindle servo block diagram

11.3.7 Defect Circuit

In the defect circuit, first the RFI signal is inverted and then bottom-held using the long and short time constants. The short time constant bottom hold responds to mirror defects of the disc above 0.1 msec, while the long time constant bottom hold holds the mirror level prior to the defect. These signals are differentiated and level-shifted by AC coupling and compared to generate the mirror defect signal. Using this signal, when the DEFECT signal is H, the tracking error is muted, and by holding the the focus error and spindle error at the value before the defect, player ability is improved.

A schematic diagram is shown in Fig. 11-13, and waveform of sections are in Fig. 11-14.

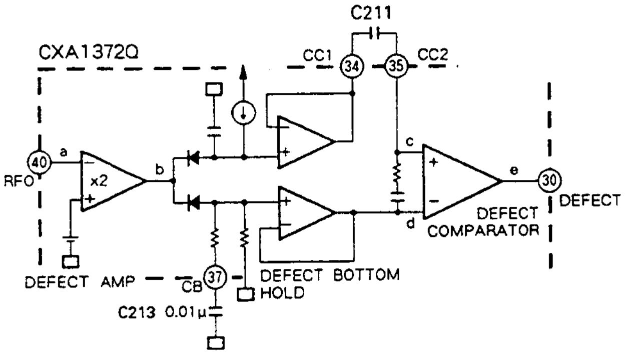

C211
CXA1372Q
CC1
34
35
CC2
40
RFO
a
x2
b
c
e
30
DEFECT
DEFECT COMPARATOR
d
DEFECT AMP
CB
37
DEFECT BOTTOM HOLD
C213 0.01μ

Fig. 11-13 DEFECT circuit

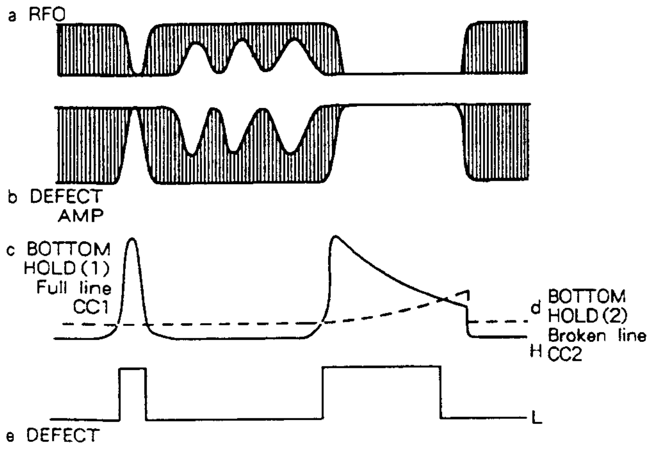


Fig. 11-14 Waveform of DEFECT circuit

11.3.8 EFM-PLL

To demodulate the played back EFM signal, for between 3T to 11T which are multiplied by T's integers to be modulated when T is taken as the channel clock period, the channel clock is required. Because inconsistencies of the spindle rotation actually change the pulse width of the EFM signal, PLL is required for playing back the channel clock.

As shown in Fig. 11-15, one of the EFM signals input to RF (Pin 24) of the CD decoder IC is passed through the internal buffer, output to ASYO (Pin 27), passed through the low pass filter composed of R266, C289, R267, and C288, and input to ASY (Pin 31) as the reference voltage of the EFM comparator of the servo control IC for CDs to compensate the asymmetry of the disc.

The other is led to the PLL inside the CD decoder IC. In this IC, as shown in Fig. 11-16, there are three stages of PLL. The first PLL is not used because it is for variable pitch playback. The second PLL generates the high frequency clock required in the third PLL, and the third PLL is a digital PLL which plays back the actual channel clocks. It is equipped with capture range of above ±150 kHz (normal state).

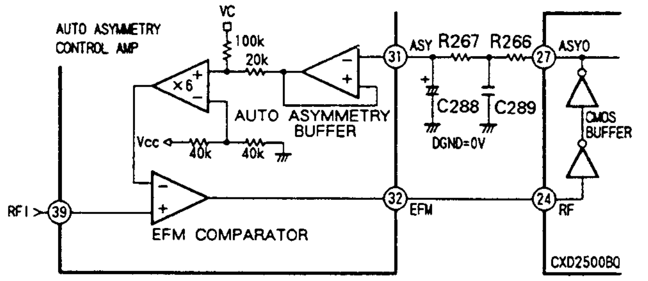

VC
AUTO ASYMMETRY CONTROL AMP
100k
20k
x6
AUTO ASYMMETRY BUFFER
Vcc
40k
40k
31
ASY
R267
R266
27
ASYO
C288
C289
DGND=0V
CMOS BUFFER
RFI
39
EFM COMPARATOR
32
EFM
24
RF
CXD2500BQ

Fig. 11-15 EFM comparator circuit

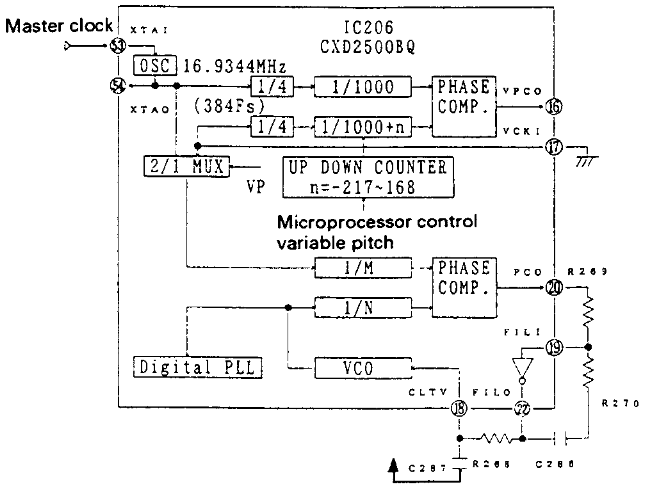

Master clock
XTAI
53
IC206
CXD2500BQ
OSC
16.9344MHz
54
XTAO
1/4
1/1000
(384Fs)
1/4
1/1000+n
PHASE COMP.
VPCO
16
VCKI
17
2/1 MUX
VP
UP DOWN COUNTER
n=-217~168
Microprocessor control variable pitch
1/M
PHASE COMP.
PCO
R269
20
1/N
FILI
19
Digital PLL
VCO
CLTV
FILO
18
22
R270
C287
R265
C286

Fig. 11-16 EFM-PLL block diagram

11.3.9 RF Detection

In the CD-R, to differentiate recorded parts from unrecorded ones, the existence of the RF signal is detected. Fig. 11-17 shows the schematic diagram of the RF detection. The mirror circuit of 11.3.10 is also shown in this figure.

First, the HF signal generated in the RF amplifier IC is passed through CN105, is led to the servo microprocessor board assembly, and is input to the HF (Pin 52) of the CDR servo amplifier IC. The outputs of the short time constant peak hold circuit (PS) and bottom hold circuit (BS) is passed through the differential amplifier, and compared with the reference voltage set externally by the comparator. When the RF signal is present, it becomes L, and absent, it becomes H, the XRFDET (Pin 61) is output, and sent to the mechanism controller.

During setup, this signal is used in the TOC area to determine if the disc has been TOC-recorded (including CDs) or not. During recording, it is used for searching for linking position and preventing double writing.

For the RF peak hold signal (RFT) used for OPC operations (optimum recording power calibration) and the RF bottom hold signal (RFB), different circuits with time constants suitable for these operations are incorporated. HF signals are also input and output to RFT (Pin 49) and RFB (Pin 47) respectively and led to the mechanism controller.

The OPC operations of this unit use the higher 4 bits of the 5-bit DA converter described in 11.3.1. After the 15-step recording, while the recorded part is played back, the difference between the RFT and RFB is calculated, and a DA converter output level is determined so that an ideal recording characteristics is obtained. The step which will produce the most ideal output voltage is selected by 5-bit accuracy (31 steps) and output, enabling recording using the ideal power.

11.3.10 Mirror Circuit

Fig. 11-17 shows the schematic diagram of the mirror circuit. The mirror circuit of this unit uses the same generation circuit as CD players for recorded parts . In unrecorded parts, a circuit unique to CD-R is utilized in which RC (radial contrast) generated by intersecting grooves is used. These circuits are switched by the RF detection signal mentioned earlier.

For unrecorded parts, the HF signal input is extracted for its RC components by the peak hold circuit (PS) with short time-constant, AC-coupled, amplified. The resultant signal is compared with integrated RC components as the reference voltage in the comparator and used as the CD-R mirror signal.

For recorded parts, the bottom hold circuit (BS) with short time constant is compared with the divided voltage of the outputs of the peak hold circuit (PL) with a long time constant and bottom hole circuit (BL) to obtain the same mirror signal as CDs.

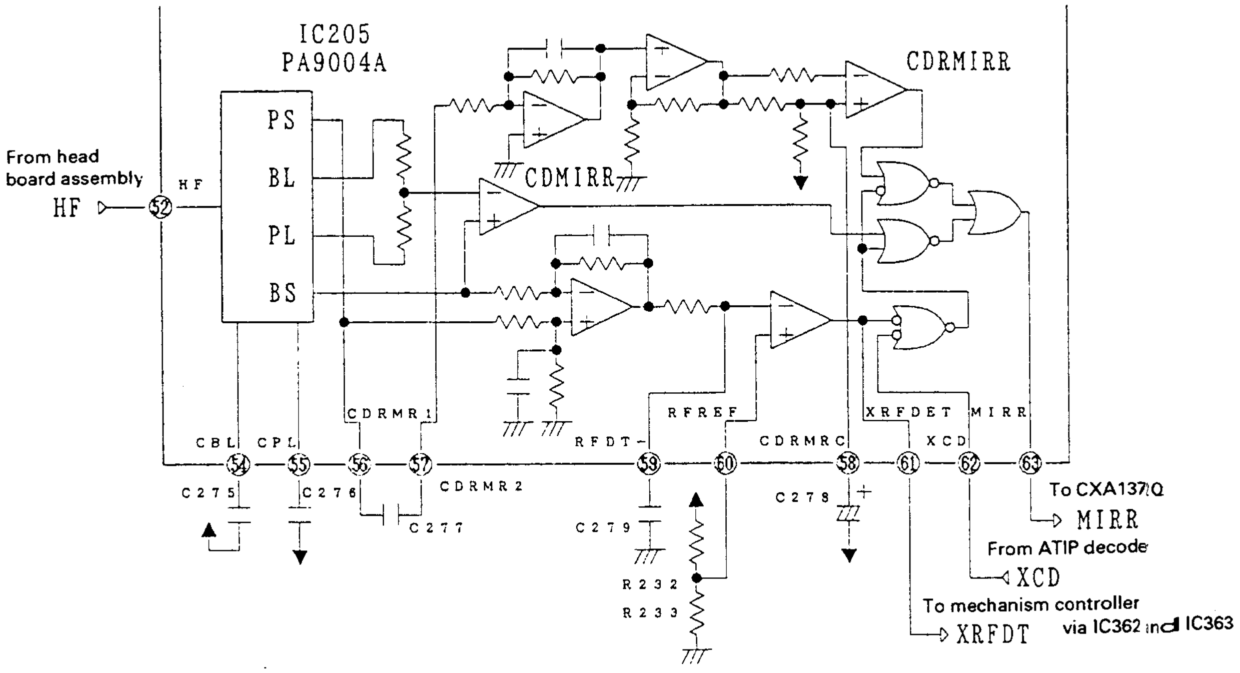


Fig. 11-17 RF detection, mirror circuit diagram

11.4 Audio Section

11.4.1 Analog Input Circuit/Recording Control

The analog signal of the Lch is input from the pin jack JA801 (1/2), input to the VR board assembly via CN801, passed through the recording balance control (VR802) and recording level control (VR801), and after balance and level are adjusted, is input to the audio digital board assembly via CN801 again. It is amplified by about 11 dB in IC803 (1/2) and led to the AD converter IC. The same is performed for the Rch analog input signal.

11.4.2 AD Converter

Fig. 11-18 shows the schematic diagram of the AD converter IC (IC801:AK5340-VS).

Only the Lch is explained here. One of the signal amplified by IC803 (1/2) is then input to AINL + (Pin 1) via R823 and the other is inverted for its phase by IC803 (2/2) and input to AINL – (Pin 2) via R819. After the differential voltage (due to inverted phase, the signal is double and the noise is half) of these signals have been adjusted, they are AD converted.

As AD converter IC control signals, the 384 fs (fs=sampling frequency) master clock is input to CLK (Pin 20) via the clock buffer (IC308), the 32 fs serial clock is input to SCLK (Pin 15), and the LR clock is input to L/R (Pin 14) from the EFM encoder IC. The fs here is 44.1 kHz, and the master clock frequency divided by 6 (64 fs) is input to CLK as an AD conversion sampling rate.

The AD converted data is output from SDATA (Pin 16) and input to the ADCDATA (Pin 33) of EFM encoder IC . Fig. 11-19 shows the relation between each clock and data.

During operation modes other than analog recording, PD (Pin 10) is made H by signals from the EFM encoder IC ADCSTBY (Pin 37) to set the power down mode. By setting this pin to L during analog recording, the AD converter IC is calibrated.

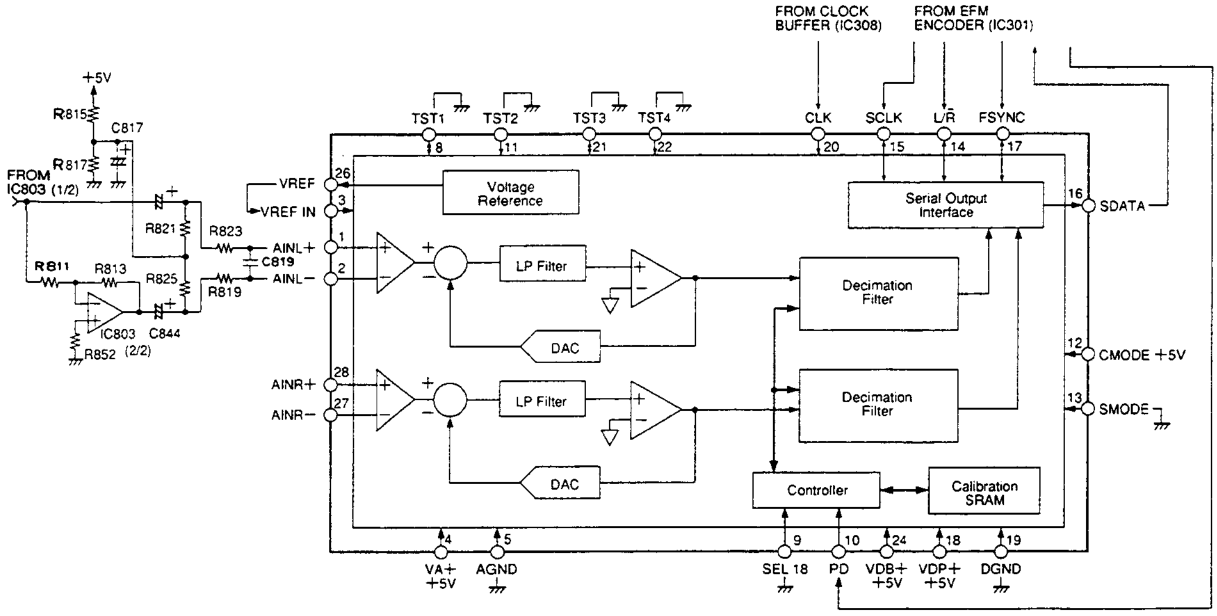

FROM CLOCK BUFFER (IC308)
FROM EFM ENCODER (IC301)
+5V
R815
C817
R817
FROM IC803 (1/2)
R821
R823
R811
R813
R825
R819
C819
IC803 (2/2)
C844
R852
VREF
VREF IN
AINL+
AINL−
AINR+
AINR−
TST1
TST2
TST3
TST4
CLK
SCLK
L/R
FSYNC
Voltage Reference
Serial Output Interface
LP Filter
DAC
Decimation Filter
Controller
Calibration SRAM
SDATA
CMODE +5V
SMODE
VA+ +5V
AGND
SEL 18
PD
VDB+ +5V
VDP+ +5V
DGND
26
3
1
2
28
27
8
11
21
22
20
15
14
17
16
12
13
4
5
9
10
24
18
19

Fig. 11-18 AD converter schematic diagram

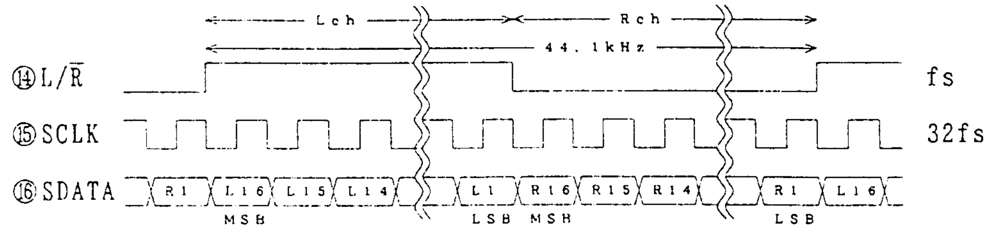

Lch
Rch
44.1kHz
⑭L/R
⑮SCLK
⑯SDATA
fs
32fs
R1
L16
L15
L14
L1
R16
R15
R14
MSB
LSB
MSB
LSB

Fig. 11-19 AD converter data output timing

11.4.3 Digital Filter

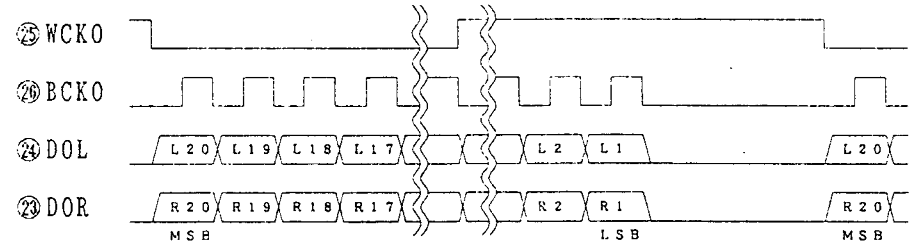
The DATA, BCK, and LRCK from the EFM encoder IC are input respectively to Pins 1, 2, and 28 of the digital filter IC (IC401 : PD7009A).

The 384 fs clock is input to XIN (Pin 6) from the clock buffer (IC308) as the master clock. × 8 oversampling 20-bit Lch and Rch data are output from DOL (Pin 24) and DOR (Pin 23) of the digital filter IC. Fig. 11-20 shows the output timing.

These digital filter ICs differ as shown in Table 11-1 according to the destination and model. Therefore use the R490, R492, R493, and R502 jumpers accordingly.

Digital Filter No.	Destination, Model	Jumper to be Used
PD7009A (Legato Link S)	PDR-05/ME8 PDR-99/KU	R490, R502
PD0116A (Legato Link)	PDR-05/J	None
SM5813AP (Normal)	PDR-05/KU	R492, R493

Table 11-1 Digital filter IC types



㉕WCKO
㉖BCKO
㉔DOL
㉓DOR
L20
L19
L18
L17
L2
L1
L20
R20
R19
R18
R17
R2
R1
R20
MSB
LSB
MSB

Fig. 11-20 Digital Filter Output Timing

11.4.4 DA Converter

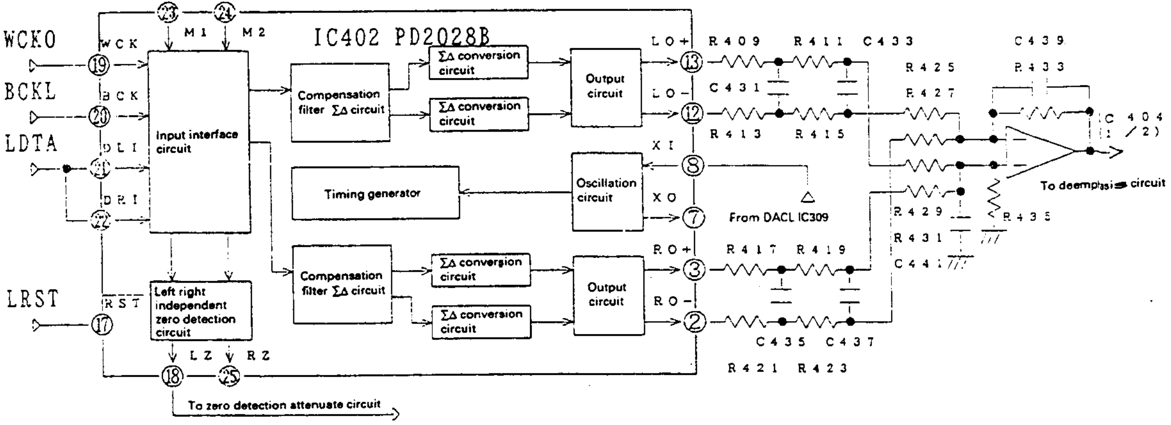
Fig. 11-21 shows the schematic diagrams of the Lch DA converter IC (IC402 : PD2028B) and differential amplifier. WCKO, BCKL, and LDTA are input from the digital filter to Pins WCK (pin 19), BCK (Pin 20), DLI (Pin 21), and DRI (Pin 22) of the DA converter IC. The 384 fs master clock is input as DACL from IC309 to XI (Pin 8).

The 8 fs data input from DLI (Pin 21) and DRI (Pin 22) is passed through the input interface and oversampled to 32 fs by the compensation filter. In the dither circuit, to prevent noise caused by idling patterns unique to the ΣΔ conversion DA converter, DC offset and dither are added to the data. The data is then oversampled to 384 fs in the sample hold circuit.

By incorporating four secondary ΣΔ conversion DA converter circuits, a 4 ΣΔ conversion circuit/ch high performance DA converter is realized.

The output circuit performs the resistance-adding of the positive phase outputs and that of the negative phase outputs from 2 ΣΔ conversion circuits and outputs them respectively from LO + and LO –. Furthermore, by operating a total of four signals (positive phase output RO + and negative phase output RO – of another channel) using an external ope-amplifier (IC404), a low distortion rate high S/N DA conversion output is obtained. This amplifier also serves as the primary low pass filter.

Likewise, the Rch is also output from the differential amplifier (IC405).



From digital filter
㉓
㉔
M1
M2
IC402 PD2028B
WCKO
WCK
⑲
BCKL
BCK
⑳
LDTA
DLI
㉑
DRI
㉒
LRST
RST
⑰
Input interface circuit
Compensation filter ΣΔ circuit
ΣΔ conversion circuit
ΣΔ conversion circuit
Output circuit
Timing generator
Oscillation circuit
Compensation filter ΣΔ circuit
ΣΔ conversion circuit
ΣΔ conversion circuit
Output circuit
Left right independent zero detection circuit
LZ
RZ
⑱
㉕
To zero detection attenuate circuit
LO+
⑬
LO–
⑫
XI
⑧
XO
⑦
RO+
③
RO–
②
From DACL IC309
R409
R411
C433
C431
R413
R415
R417
R419
C435
C437
R421
R423
R425
R427
R429
R431
C441
C439
R433
R435
C404
(1/2)
To deemphasis circuit

Fig. 11-21 DA converter schematic diagram

11.4.5 Analog Output Circuit

Fig. 11-22 shows the schematic diagram of the Lch output buffer. The output of IC404 (1/2) mentioned earlier is input to the IC404 (2/2) inverted input pin via R437, R483, and R447. C447, C449, R483, R447, and R445 make up the secondary low pass filter here. This section has the following three functions.

First, it serves as a deemphasis circuit. When a preemphasized software is run, the control signal DEEMP is set to H and the transistor Q411 turns on. At this time, deemphasis is imposed by R437, R477, and C465.

Secondly, it serves as a muting circuit. When the POWER switch is turned on/off, and when the input selector is switched, the control signal MUTE is set to H, and the muting transistor Q407 is turned on to mute the audio output.

Thirdly, it serves as a zero detection attenuate circuit. It improves the S/N when the data input to the DA converter IC is all zero (when no signals). When the DA converter detects the no-signal state, the control signal LZ is set to H and the attenuate transistor Q409 is turned on to attenuate the noise level of the audio output.

The outputs of this circuit are fed to the rear panel pin jack (JA401) and amplified by headphone amplifier IC (IC406) and fed to the headphone board assembly.

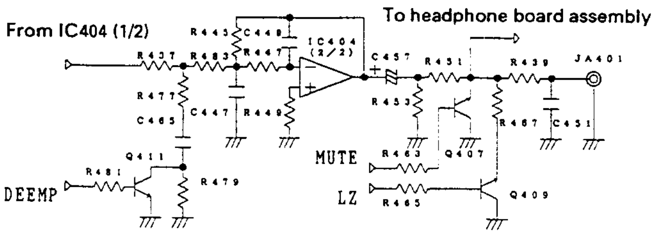


Fig. 11-22 Deemphasis, muting, zero detection attenuate schematic diagram

11.5 Digital Audio Section

11.5.1 Digital Audio Interface Demodulation (DIR) Block

This unit has two digital inputs-coaxial (COAX) and optical (OPT). The COAX input is waveform-shaped by the two inverters of IC307 and Schmidt inverter of IC312, and input to Pin 4 of the EFM encoder IC. The OPT input is photoelectric converted by the optical reception module (JA301) and input to Pin 1 of the EFM encoder IC. To prevent the effects of noises during COAX input, the power of the optical reception module is turned off.

Fig. 11-23 shows the schematic diagram of the DIR (digital audio interface receiver) in the EFM encoder IC. The inputs from Pins 1 and 4 are selected by the input selection circuit and bi-phase-demodulated. To create the reference clock for extracting data, the edge of the input data is detected and sent to the phase comparator of the PLL. Next, preamble detection and parity error check are performed, and the results are used to determine lock. When locked, L is output from DIRERR (Pin 20) and input to of the servo microprocessor board assembly (the mode controller (IC351 : PD4591A).) When unlock, H is output. For lockup to be performed smoothly, the temporary reference time (frequency close to fs) is created by the RC oscillator composed of DIRRC1 (Pin 5) and DIRRC2 (Pin 6).

Next, clocks are generated by the clock generator and the audio data, C bit, and U bit are extracted. The audio data, bit clock, and LR clock are each output from DIRDATA (Pin 17), DIRBCK (Pin 15), and DIRLRCK (Pin 16) respectively, and input to the FS converter IC as well as to the data selector in the EFM encoder IC. Fig. 11-24 shows the audio data output timing. The C bit and U bit data are sent to the mode controller via the microprocessor I/F. This IC is equipped with a function which sends U bit to the microprocessor I/F in the optimum form according to the category code detected from C bit. However, these data are not output when unlocked.

The PLL is composed of the phase comparator, LPF, VCO, and frequency divider. The phase comparator perform phase comparison at 64 fs using the reference clock made from the input signal and the clock obtained by frequency-dividing the VCO. The output is then smoothed by the DIRLPF (Pin 11) LPF and input to VCO as the control voltage. The VCO is generated at 384 fs by the DIRVCO (Pin 10) freerunning setting resistor and DIRRS (Pin 8) oscillation band adjustment resistor.

On the other hand, the selected signal is sent to the digital audio interface modulation block as the through output.

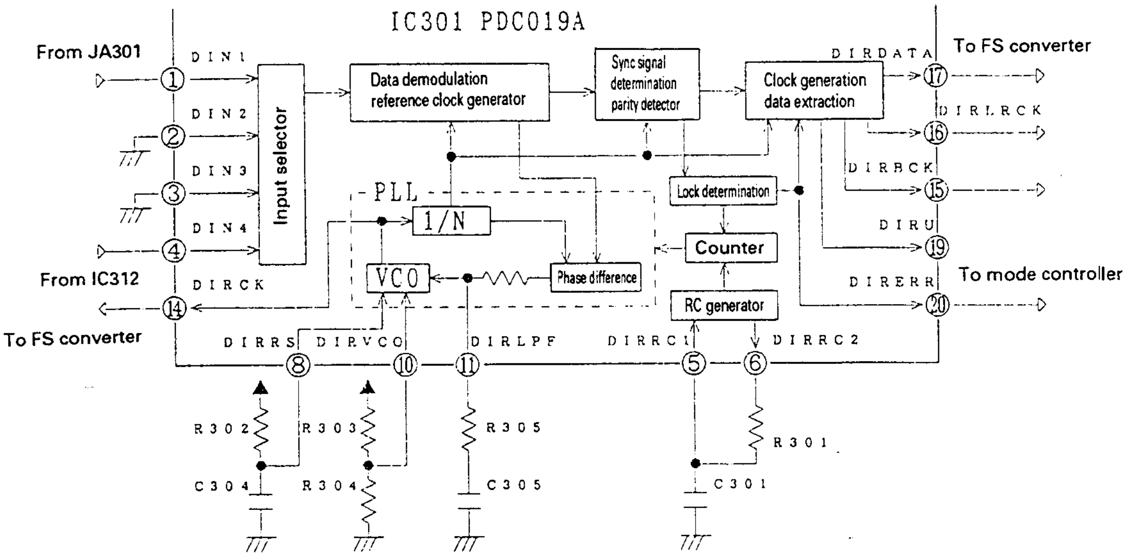

IC301 PDC019A
From JA301
DIN1
DIN2
DIN3
DIN4
①
②
③
④
From IC312
DIRCK
⑭
To FS converter
Input selector
Data demodulation reference clock generator
Sync signal determination parity detector
Clock generation data extraction
PLL
1/N
VCO
Phase difference
Lock determination
Counter
RC generator
DIRDATA
To FS converter
⑰
DIRLRCK
⑯
DIRBCK
⑮
DIRU
⑲
DIRERR
To mode controller
⑳
DIRRS
DIRVCO
DIRLPF
DIRRC1
DIRRC2
⑧
⑩
⑪
⑤
⑥
R302
R303
R305
R301
C304
R304
C305
C301

Fig. 11-23 DIR block schematic diagram

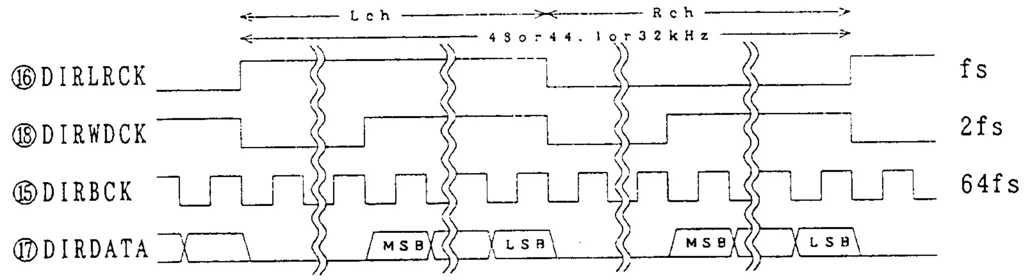

Lch
Rch
48 or 44.1 or 32 kHz
⑯DIRLRCK
⑱DIRWDCK
⑮DIRBCK
⑰DIRDATA
MSB
LSB
MSB
LSB
fs
2fs
64fs

Fig. 11-24 DIR section audio data output timing

11.5.2 FS Converter

Fig. 11-25 shows a schematic diagram of the FS converter IC (IC306 : PDC020A)

The digital input audio data demodulated by the EFM encoder IC is input to LRCKI (Pin 8), BCKI (Pin 4), and DATAI (Pin 9). For digital inputs with sampling frequency of 48 kHz or 32 kHz, audio data is converted into 44.1 kHz, and for 44.1 kHz, the internal circuits are all passed before output.

As for the conversion method, the 48 kHz or 32 kHz data is first × 8 oversampled by the digital filter. The process is carried out by the 384 fs clock input to MCK1 (Pin3). Data required for the 44.1 kHz output timing is then extracted from this data, and the output data is calculated by compensation calculation using the data from the internal coefficient ROM. The internal PLL clock is used here. The PLL VCO is oscillated at 14.112 MHz. In the phase comparator, the clock frequency-divided by 294 (when the fs is 48 kHz) and the clock frequency-divided by 441 (when fs is 32 kHz) are compared with the LR clock input to control the VCO.

The converted data is output to LRCKO (Pin 26), BCLKO (Pin 28), and DATAO (Pin 25), and input to the EFM encoder IC again. The timing of the output data is as shown in Fig. 11-24 except that the sampling frequency is 44.1 kHz. The internal operating mode is set by the 8-bit data by serial communication from the mode controller. This data is output as DO0 to DO7 to the external terminal. DO0 to DO4 are used for internal settings and DO5 to DO7 as general resistors. Table 11-2 shows the details.

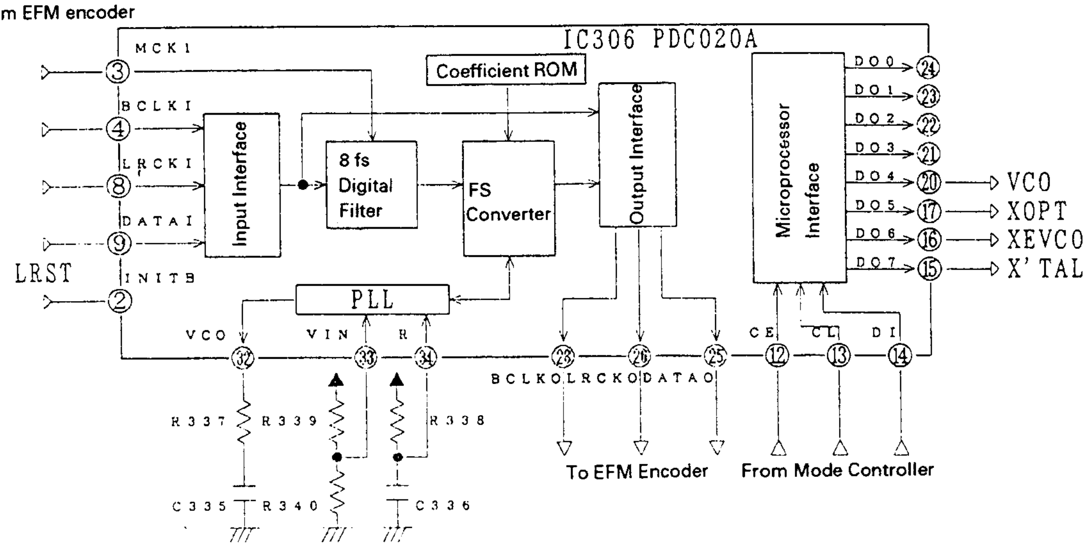

From EFM encoder
IC306 PDC020A
MCKI
③
BCLKI
④
LRCKI
⑧
DATAI
⑨
LRST
INITB
②
Coefficient ROM
Input Interface
8 fs Digital Filter
FS Converter
Output Interface
Microprocessor Interface
PLL
DO0 ㉔
DO1 ㉓
DO2 ㉒
DO3 ㉑
DO4 ⑳ VCO
DO5 ⑰ XOPT
DO6 ⑯ XEVCO
DO7 ⑮ X'TAL
VCO ㉜
VIN ㉝
R ㉞
㉘ ㉖ ㉕
BCLKO LRCKO DATAO
CE ⑫
CL ⑬
DI ⑭
R337
R339
R338
C335
R340
C336
To EFM Encoder
From Mode Controller

Fig. 11-25 FS converter schematic diagram

Register Output Pin	Signal Name	Details
DO0	MKSEL	Internal digital filter clock selection L: 384 fs, H: 512 fs
DO1	FSEL1	Sampling frequency selection. L: 44.1 kHz, H: Other than 44.1 kHz
DO2	FSEL2	Sampling frequency selection. L: 48 kHz. H: 32 kHz
DO3	MUTE	Output data mute. L: OFF. H: Soft mute
DO4	STOP	FS converter VCO and jitter absorption buffer VCO oscillation control. L: Stop. H: Oscillation
DO5	XOPT	Optical module JA301 power supply control. L: ON. H: OFF
DO6	XEVCO	EFM encoder VCO generation control. L: Oscillation. H: Stop
DO7	X'TAL	Master clock selection. L: VCO. H: Crystal

Table 11-2 FS converter IC register details

11.5.3 Clock Jitter Suppressor (CJS) Block

To input the data and clock from the FS converter IC to the DA converter IC, it is necessary to reduce the jitter as much as possible. In this block, by imposing another trigger using a jitter-less clock made by a VCO (lithium tantlate) with highly stable frequency compared to normal VCOs, clean clocks and data are supplied to the following circuits.

Operations are explained according to the schematic diagram of Fig. 11-26. The FS converter output is input to CJSLRCK (Pin 24), CJSBCK (Pin 23), and CJSDATA (Pin 22).

The 16.934 MHz output from VOUT (Pin 8) of the VCO PCX1021 (IC303) is input to JITVCOIN (Pin 25) of the EFM encoder IC, and using CJSLRCK and the LRCK created by frequency-dividing this, phase comparison is performed. When the difference in phase between these two LRCKs is above 90 degrees, it is determined as unlocked and mute is imposed. The phase comparison output is output to JITPCO (Pin 28), passes through the JITLPFI (Pin 27) and JITLPFO (Pin 26) filters and input to VIN (Pin 1) of the VCO to control the oscillation frequency.

The inputs from the FS converter IC imposed with re-trigger by the VCO clock are fed to the data selector in the EFM encoder IC.

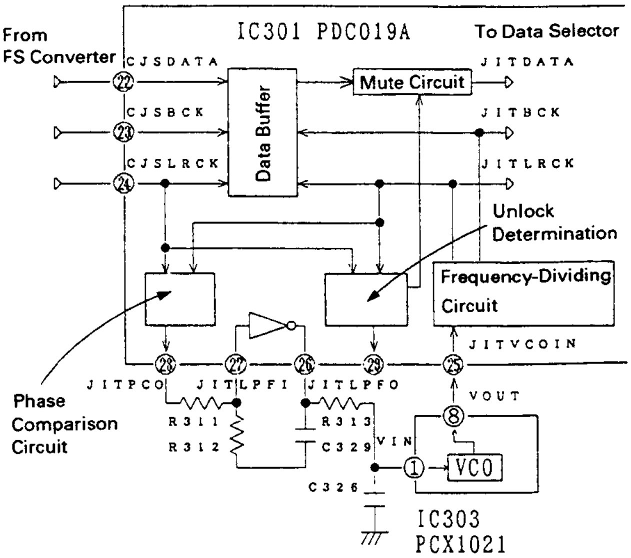

From FS Converter
IC301 PDC019A
To Data Selector
CJSDATA
㉒
CJSBCK
㉓
CJSLRCK
㉔
Data Buffer
Mute Circuit
JITDATA
JITBCK
JITLRCK
Unlock Determination
Frequency-Dividing Circuit
JITVCOIN
㉘ ㉗ ㉖ ㉙ ㉕
Phase Comparison Circuit
JITPCO
JITLPFI
JITLPFO
VOUT
⑧
R311
R312
R313
C329
VIN
①
VCO
C326
IC303
PCX1021

Fig. 11-26 Clock jitter suppressor circuit

11.5.4 Data Selector, Digital Fader, Level Meter, Mute Block

The outputs from the DIR block, AD converter IC, CD decoder IC, and CJS block are selected by the data selector block by the commands from the mode controller, and input to the digital fader and level meter.

In the digital fader block, fade in and fade out operations are performed during recording and playback by the attenuation data from the mode controller.

In the level meter block, absolute value conversion and logarithmic conversion are performed for the data input, the peak-held 8-bit data is read by the mode controller from the microprocessor I/F to light up the front panel level meter. Furthermore, absolute zero level detection is performed and used for detection no-sound states during the recording of the digital input.

The digital fader outputs are passed through the mute block, and one is output to DACDATA (Pin 30), DACBCK (Pin 31), and DACLRCK (Pin 32) as the output to the DA converter IC, and the other is led to the memory controller block in the EFM encoder IC.

11.5.5 Memory Controller Block

The memory controller is equipped with a function which delays the audio data for recording. The 16-bit data is serial/parallel-converted every 4 bits and is delayed by about 700 ms by the external 1Mbit DRAM. The DRAM used here (IC304 : MB81C4256A) corresponds to the fast page mode and is refreshed every 11.6 ms. This block is used for preventing the head of data from dropping immediately after recording starts according to the copy prohibition bit determination time and disc rotation standby time during digital input recording.

For the writing clock of this block, the same clock output to the DA converter IC is used. The reading clock is created by the clock created at the external VCO (IC302 : CD74HC4046AM).

The data output from this block is fed to the CD encode block in the EFM encoder IC.

11.5.6 EFM Encoder Block

Fig. 11-27 shows the schematic diagram of the EFM encoder block and its peripherals. The audio data output from the memory controller block is interleaved by the CIRC (Cross Interleave Reed-Solomon Code) encoder, added with the C1 and C2 error correction codes, EFM-modulated (Eight to Fourteen Modulations), and added with subcodes, sync, and merge bits. It is then NRZI-converted to become the CD format EFM signal. This IC incorporates a CIRC encoder RAM.

3T to 11T (T = 231 nsec) signals are created here, which are the signals on the disc. To obtain the ideal length when the bit length is played back after recording, the LD power On time is slightly reduced by the strategy block. Specifically, the 3T to 11T pulse is made (N-1)T, taken as 2T to 10T, and 2T is converted to a longer pulse of 60 nsec and 3T to 10 nsec. This output is finally output from Pin 3 of IC310, passes through the servo microprocessor board assembly, passes through CN105, converted to the recording pulse by the LD driver circuit of the head board assembly, and recorded on the disc by driving the pickup LD.

The CD-R recorders perform laser power calibration before recording. The test signal for this is also created in this block, switched with the audio data EFM signal during calibration, and output.

As this IC also controls the start of the output of the EFM signal using the RF detection signal input to XRFDET (Pin 83), it is able to additionally record at an accurate timing.

As EFM encoder processing requires EFM master clocks, PLL is composed of the internal phase comparator, LPF, external VCO (IC302). In the phase comparator, using the LR clock of the writing side of the memory controller block as reference, the clock (17.2872 MHz) divided by 392 input to ENCVCOIN (Pin 76) from the VCO is compared with the reference, and output from ENCPCO (Pin 79). The signal is then passed through the ENCLPFI (Pin 78) and ENCLPFO (Pin 77) LPF, input to VCOIN (Pin 9) of the VCO to control the oscillation frequency.

To synchronize the subcode sync of the EFM signal to be recorded and the ATIP sync on the disc, the ATIP sync from the ATIP decoder IC is input to the ATIPSYNC (Pin 94). This is valid when XEXTSYNC (Pin 93) is L and is synchronized while standing by for recording. Subcode sync of the EFM signal for confirmation is output from the SUBSYNC (Pin 95) and taken into the mechanism controller.

The microprocessor I/F connected to the mode controller and mechanism controller via four lines-CE (Pin 97), CL (Pin 98), DI (Pin 99), and DO (Pin 100). Via this I/F, EFM encoder IC internal operation mode settings, digital out C bit setting, digital fader attenuate data input, subcode P and Q input, bits C and U read from digital input signal output, PLL lock conditions output, and level meter data output.

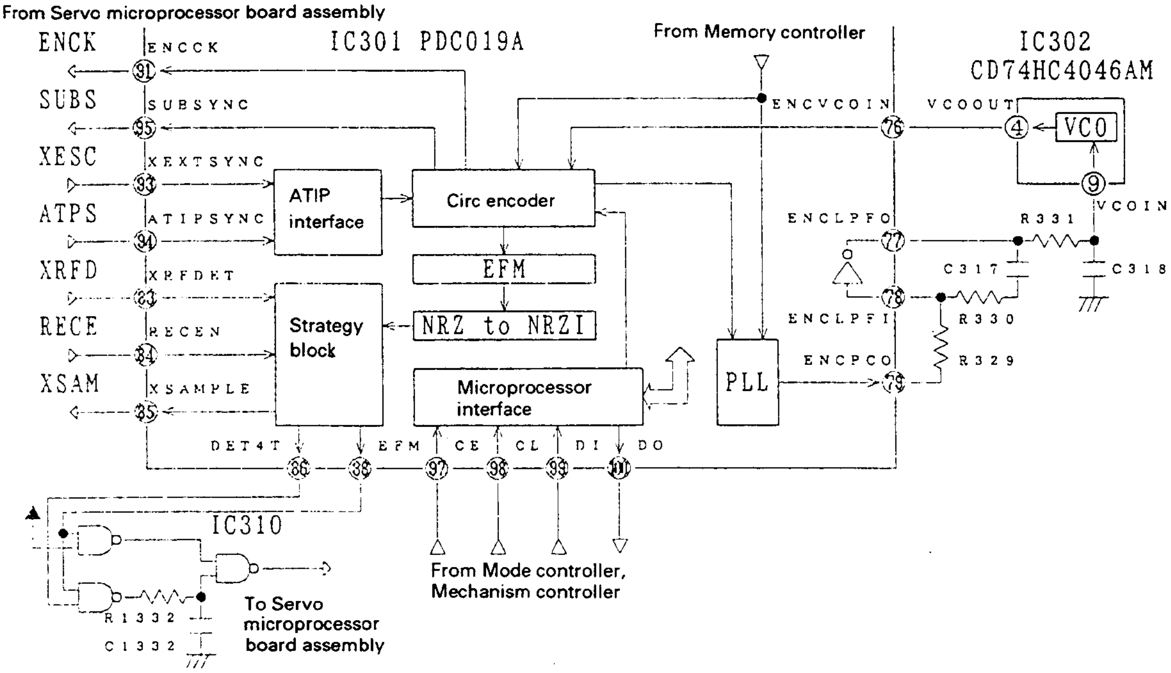

From Servo microprocessor board assembly
ENCK
ENCCK
IC301 PDC019A
From Memory controller
IC302
CD74HC4046AM
SUBS
SUBSYNC
ENCVCOIN
VCOOUT
VCO
XESC
XEXTSYNC
ATIP interface
Circ encoder
ATPS
ATIPSYNC
ENCLPFO
R331
VCOIN
XRFD
XRFDET
EFM
C317
C318
RECE
RECEN
Strategy block
NRZ to NRZI
ENCLPFI
R330
XSAM
XSAMPLE
Microprocessor interface
PLL
ENCPCO
R329
DET4T
EFM
CE
CL
DI
DO
IC310
From Mode controller, Mechanism controller
R1332
C1332
To Servo microprocessor board assembly

Fig. 11-27 EFM Encoder block and peripherals schematic diagram

11.5.7 Digital Audio Interface Modulation (DIT) Block

There are three digital audio interface outputs-through signal from the digital audio interface input, playback signal from a disc encoded at the CD decoder IC, and analog input AD-converted and encoded. These are selected inside the EFM encoder IC according to each mode, passed through JA302 as the coaxial output and JA303 as the optical output from DITOUT (Pin 48), and sent to outside.

In this block, DATA from the AD converter are especially converted to the digital audio interface format. At this time, C bit is set via the microprocessor I/F and output as category: CD, sampling frequency:44.1 kHz, emphasis:none, copy prohibit, clock accuracy as ±1000 ppm.

11.5.8 Master Clock

During recording of digital inputs with 48 or 32 kHz fs, a clock 384 times the fs created at the DIR block VCO is output from DIRCK (Pin 14). This clock is input to MCK1 (Pin 3) as the master clock of the digital filter of the FS converter IC. The clock frequency-divided inside serves as the reference for the FS converter PLL. A 14.112 MHz, which is 294 times the fs (441 times when 32 kHz) is created and is used as the master clock of the FS converter.

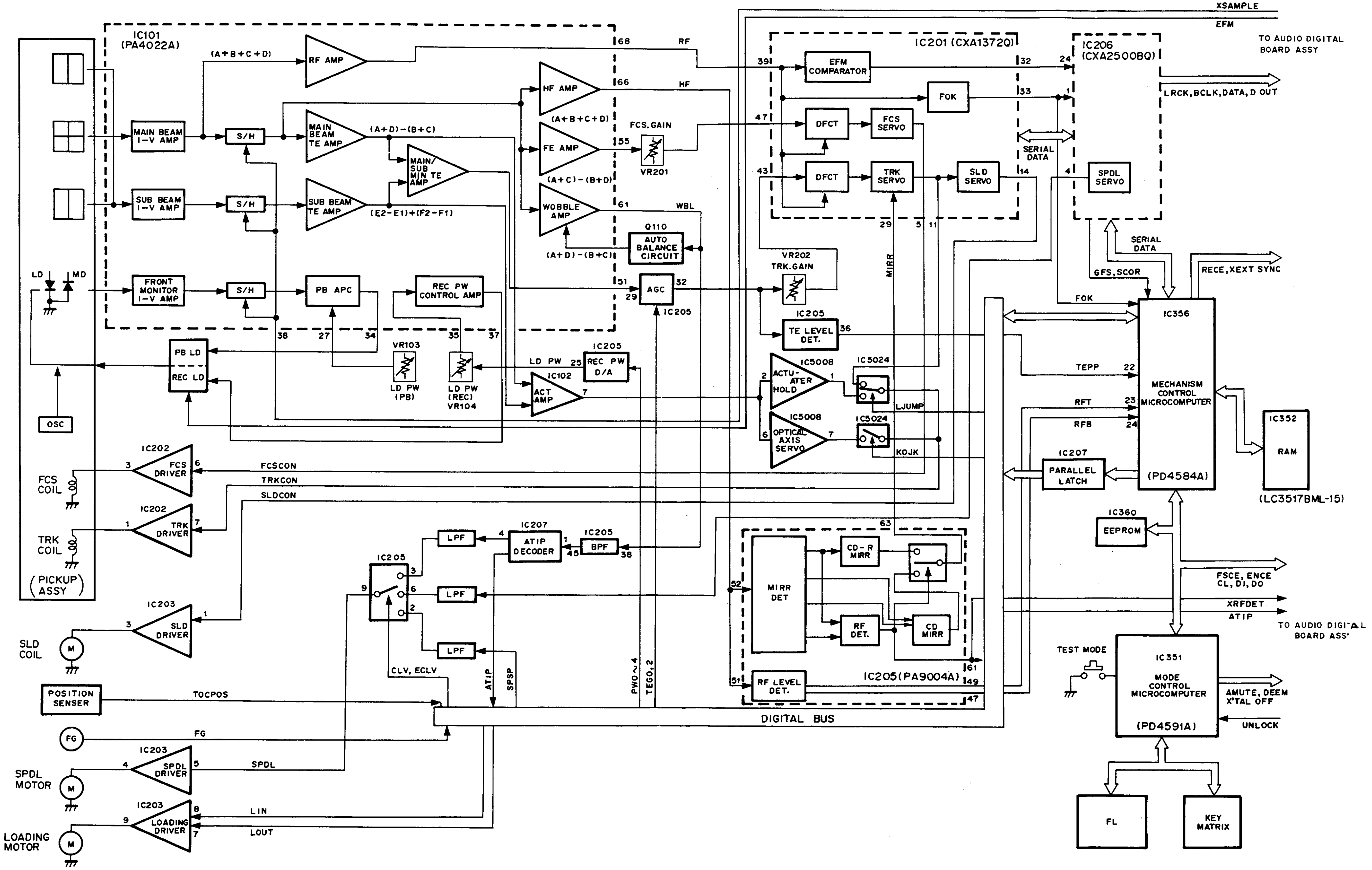
The LR clock output from the LRCKO (Pin 26) of the FS converter IC is input from CJSLRCK (Pin 24) as the reference clock of the CJS section. PLL is further composed by the lithium tantlate VCO. When the digital input fs is 44.1 kHz, the output from DIR serves as the reference clock as it is. The lithium tantlate is oscillated at 16.934 MHz, which is 384 times the 44.1 kHz clock, and is used as the master clock during digital inputs in blocks hereafter.

During recording of the analog input and disc playback, the 16.934 MHz of the IC308 crystal oscillator serves as the master clock of the system. The oscillation of the VCO of the DIR section and VCO of the CJS section stops.

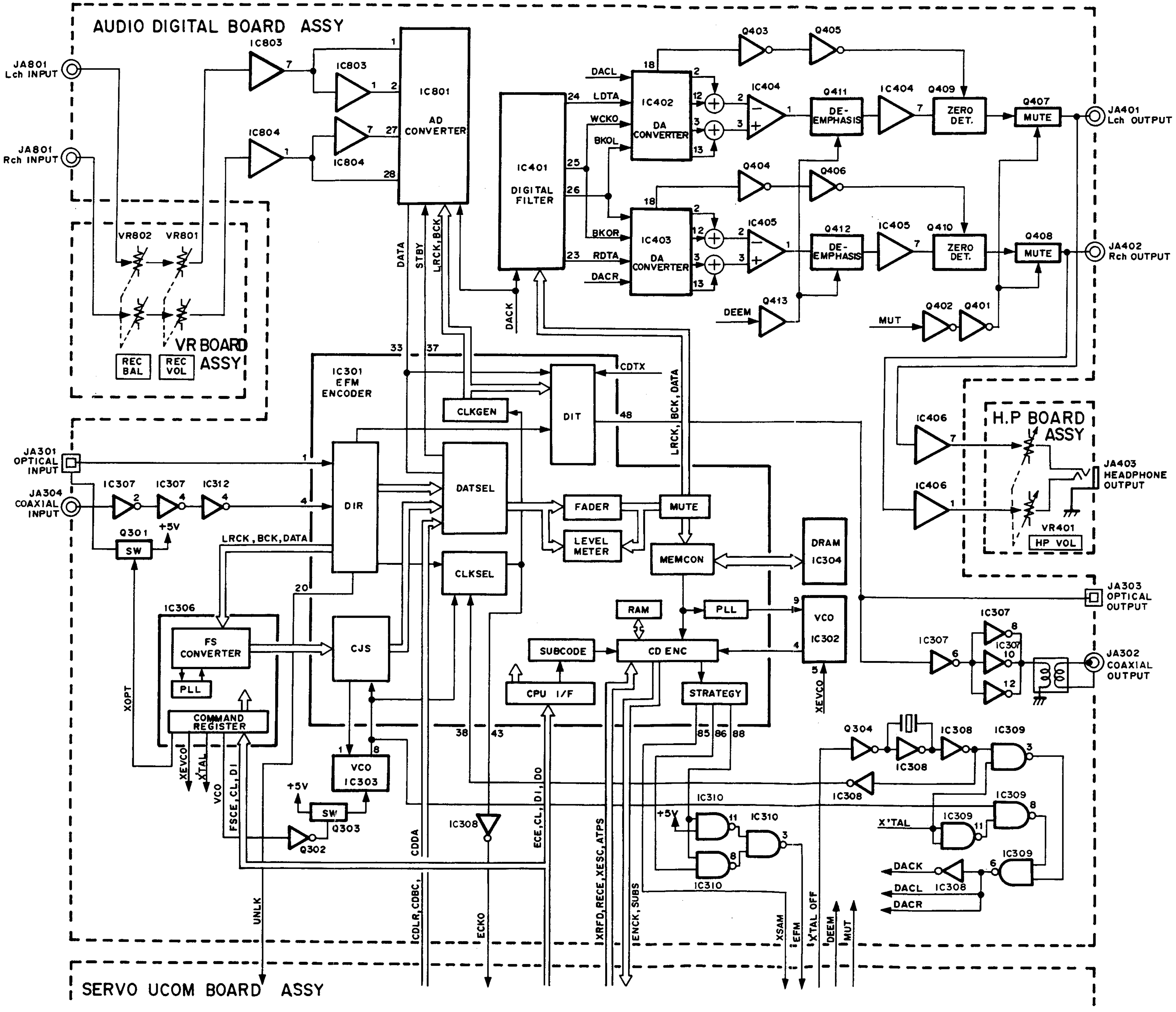
The above two 16.9344 MHz master clocks are selected by IC309 according to the operation mode of this unit. The master clock selected here is supplied to the EFM encoder IC, CD decoder IC, AD converter IC, digital filter IC, and DA converter IC.

12. BLOCK DIAGRAMS

12.1 SERVO SYSTEM


IC101
(PA4022A)
(A+B+C+D)
RF AMP
HF AMP
(A+B+C+D)
FE AMP
(A+C)-(B+D)
WOBBLE AMP
(A+D)-(B+C)
MAIN BEAM I-V AMP
SUB BEAM I-V AMP
FRONT MONITOR I-V AMP
S/H
MAIN BEAM TE AMP
(A+D)-(B+C)
MAIN/SUB MIN TE AMP
SUB BEAM TE AMP
(E2-E1)+(F2-F1)
PB APC
REC PW CONTROL AMP
LD
MD
OSC
PB LD
REC LD
VR103
LD PW (PB)
LD PW (REC) VR104
LD PW
IC102
ACT AMP
IC205
REC PW D/A
FCS.GAIN
VR201
Q110
AUTO BALANCE CIRCUIT
AGC
IC205
RF
HF
WBL
68
66
55
61
51
29
32
38
27
34
35
37
25
7
IC201 (CXA1372Q)
EFM COMPARATOR
FOK
DFCT
FCS SERVO
DFCT
TRK SERVO
SLD SERVO
39
47
43
32
33
14
29
5
11
VR202
TRK.GAIN
IC205
TE LEVEL DET.
36
IC5008
ACTU-ATER HOLD
IC5008
OPTICAL AXIS SERVO
IC5024
IC5024
LJUMP
KOJK
MIRR
IC206
(CXA2500BQ)
SPDL SERVO
SERIAL DATA
SERIAL DATA
GFS, SCOR
FOK
XSAMPLE
EFM
TO AUDIO DIGITAL BOARD ASSY
LRCK, BCLK, DATA, D OUT
RECE, XEXT SYNC
IC356
MECHANISM CONTROL MICROCOMPUTER
(PD4584A)
TEPP
RFT
RFB
22
23
24
IC352
RAM
(LC3517BML-15)
IC207
PARALLEL LATCH
IC360
EEPROM
FSCE, ENCE
CL, DI, DO
XRFDET
ATIP
TO AUDIO DIGITAL BOARD ASSY
TEST MODE
IC351
MODE CONTROL MICROCOMPUTER
(PD4591A)
AMUTE, DEEM
X'TAL OFF
UNLOCK
FL
KEY MATRIX
IC202
FCS DRIVER
FCS COIL
FCSCON
TRKCON
SLDCON
IC202
TRK DRIVER
TRK COIL
(PICKUP ASSY)
IC203
SLD DRIVER
SLD COIL
POSITION SENSER
TOCPOS
FG
IC203
SPDL DRIVER
SPDL MOTOR
SPDL
IC203
LOADING DRIVER
LOADING MOTOR
LIN
LOUT
IC205
LPF
LPF
LPF
CLV, ECLV
IC207
ATIP DECODER
IC205
BPF
ATIP
SPSP
PWO~4
TEGO,2
63
CD-R MIRR
MIRR DET
RF DET.
CD MIRR
RF LEVEL DET.
IC205 (PA9004A)
52
51
61
49
47
DIGITAL BUS

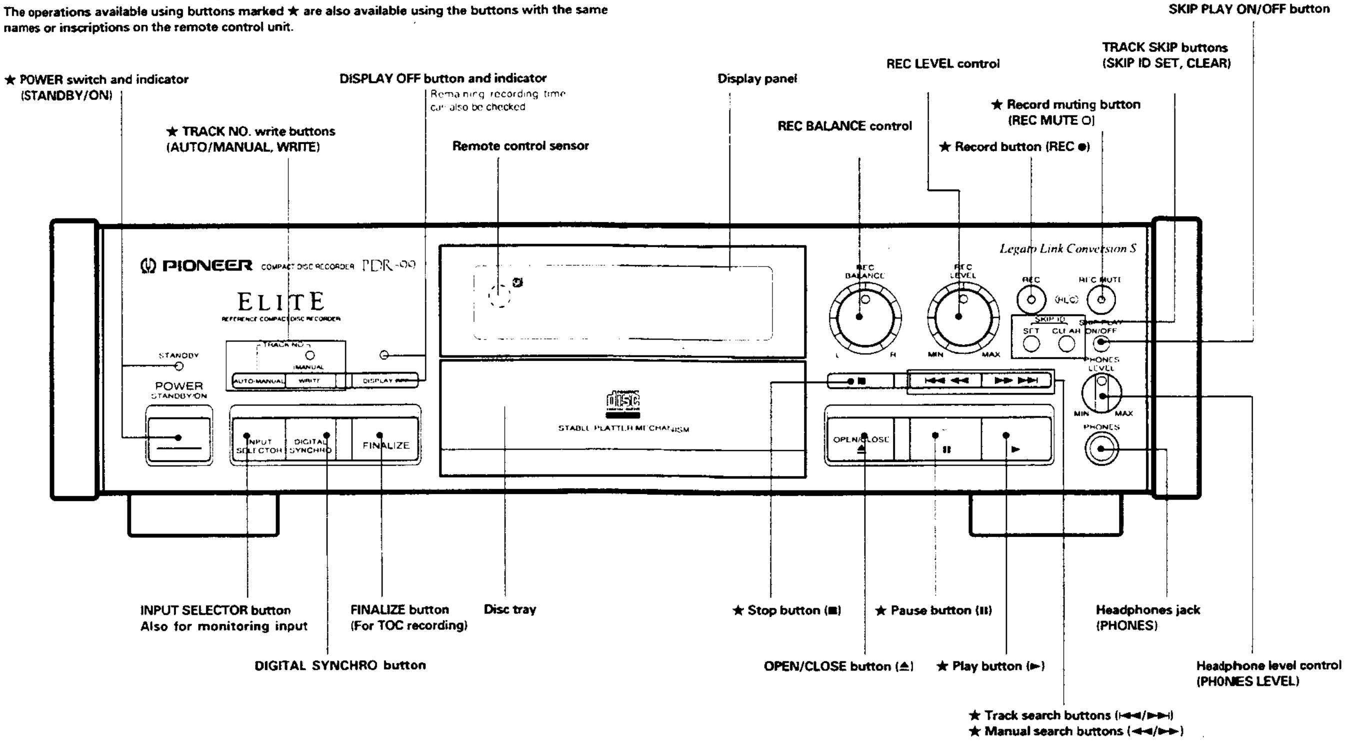
12.2 AUDIO SYSTEM


AUDIO DIGITAL BOARD ASSY
JA801 Lch INPUT
JA801 Rch INPUT
IC803
IC804
IC801 AD CONVERTER
VR802
VR801
VR BOARD ASSY
REC BAL
REC VOL
DATA
STBY
LRCK, BCK
DACK
IC401 DIGITAL FILTER
DACL
LDTA
WCKO
BKOL
BKOR
RDTA
DACR
IC402 DA CONVERTER
IC403 DA CONVERTER
IC404
IC405
Q403
Q405
Q404
Q406
Q411 DE-EMPHASIS
Q412 DE-EMPHASIS
Q409 ZERO DET.
Q410 ZERO DET.
Q407 MUTE
Q408 MUTE
DEEM
Q413
MUT
Q402
Q401
JA401 Lch OUTPUT
JA402 Rch OUTPUT
IC406
H.P BOARD ASSY
JA403 HEADPHONE OUTPUT
VR401
HP VOL
IC301 EFM ENCODER
CDTX
DIT
CLKGEN
LRCK, BCK, DATA
JA301 OPTICAL INPUT
JA304 COAXIAL INPUT
IC307
IC312
+5V
Q301
SW
DIR
DATSEL
CLKSEL
FADER
LEVEL METER
MUTE
MEMCON
DRAM IC304
IC306
FS CONVERTER
PLL
COMMAND REGISTER
CJS
XOPT
XEVCO
XTAL
VCO
FSCE, CL, DI
VCO IC303
Q303
Q302
RAM
PLL
VCO IC302
SUBCODE
CD ENC
CPU I/F
STRATEGY
XEVCO
JA303 OPTICAL OUTPUT
JA302 COAXIAL OUTPUT
Q304
IC308
IC309
IC310
X'TAL
DACK
DACL
DACR
IC308
CDDA
ECE, CL, DI, DO
XRFD, RECE, XESC, ATPS
ENCK, SUBS
UNLK
CDLR, CDBC,
ECKO
XSAM
EFM
XTAL OFF
DEEM
MUT
SERVO UCOM BOARD ASSY

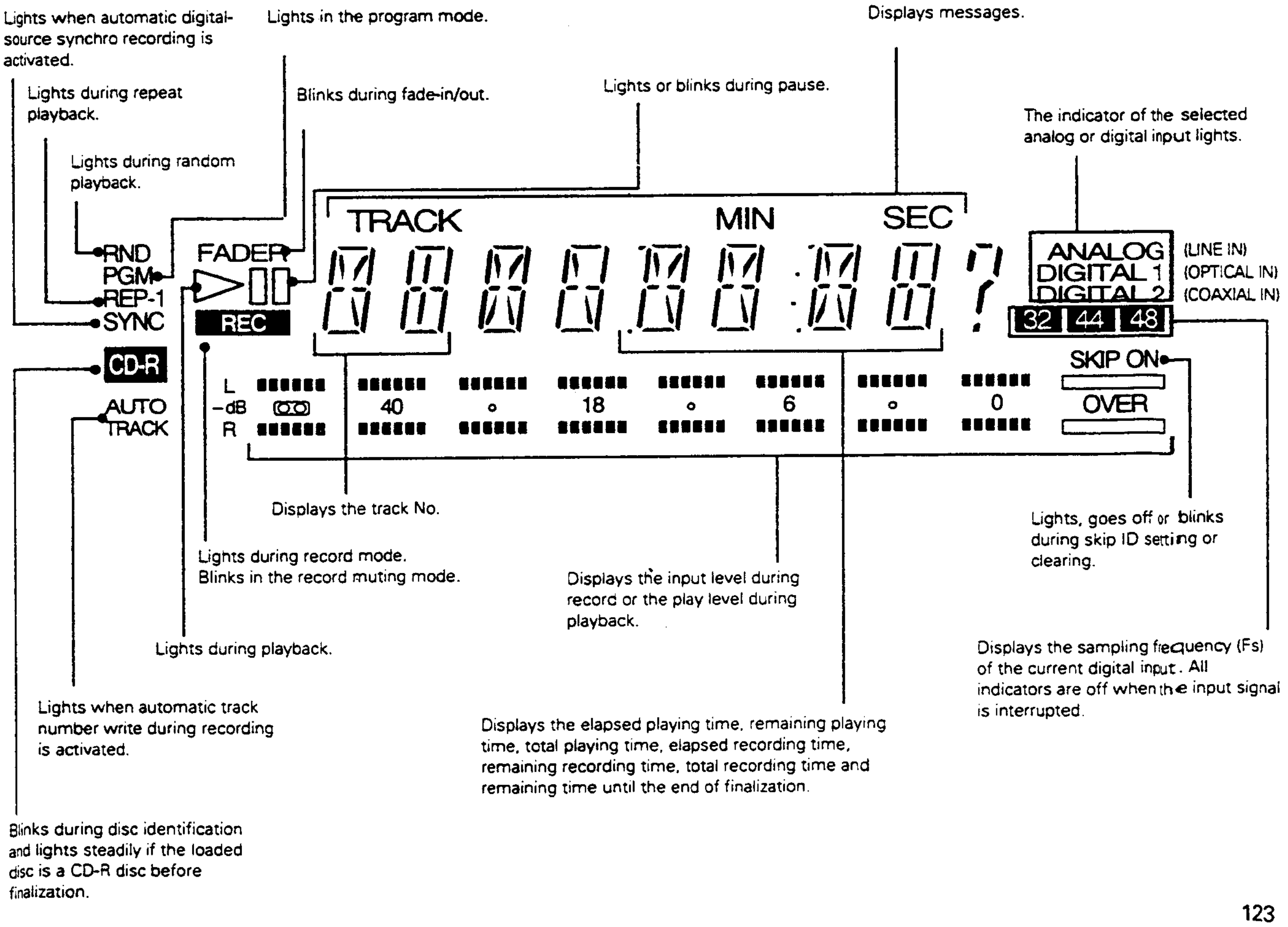
13. PANEL FACILITIES

• FRONT PANEL (For PDR-99)

The operations available using buttons marked ★ are also available using the buttons with the same names or inscriptions on the remote control unit.


SKIP PLAY ON/OFF button
TRACK SKIP buttons (SKIP ID SET, CLEAR)
REC LEVEL control
★ POWER switch and indicator (STANDBY/ON)
DISPLAY OFF button and indicator
Remaining recording time can also be checked
Display panel
★ Record muting button (REC MUTE ○)
★ TRACK NO. write buttons (AUTO/MANUAL, WRITE)
REC BALANCE control
Remote control sensor
★ Record button (REC ●)
PIONEER
COMPACT DISC RECORDER PDR-99
ELITE
REFERENCE COMPACT DISC RECORDER
Legato Link Conversion S
REC BALANCE
REC LEVEL
REC
REC MUTE
(HLC)
SKIP ID
SET
CLEAR
SKIP PLAY ON/OFF
TRACK NO.
MANUAL
AUTO·MANUAL
WRITE
DISPLAY OFF
STANDBY
POWER STANDBY/ON
L
R
MIN
MAX
PHONES LEVEL
PHONES
INPUT SELECTOR
DIGITAL SYNCHRO
FINALIZE
STABLE PLATTER MECHANISM
OPEN/CLOSE
INPUT SELECTOR button Also for monitoring input
FINALIZE button (For TOC recording)
Disc tray
★ Stop button (■)
★ Pause button (II)
Headphones jack (PHONES)
DIGITAL SYNCHRO button
OPEN/CLOSE button (≜)
★ Play button (►)
Headphone level control (PHONES LEVEL)
★ Track search buttons (⏮/⏭)
★ Manual search buttons (◀◀/▶▶)

• DISPLAY


Lights when automatic digital-source synchro recording is activated.
Lights in the program mode.
Displays messages.
Lights during repeat playback.
Blinks during fade-in/out.
Lights or blinks during pause.
The indicator of the selected analog or digital input lights.
Lights during random playback.
TRACK
MIN
SEC
RND
PGM
REP-1
SYNC
FADER
REC
ANALOG (LINE IN)
DIGITAL 1 (OPTICAL IN)
DIGITAL 2 (COAXIAL IN)
32
44
48
CD-R
SKIP ON
AUTO TRACK
L
-dB
R
40
18
6
0
OVER
Displays the track No.
Lights, goes off or blinks during skip ID setting or clearing.
Lights during record mode. Blinks in the record muting mode.
Displays the input level during record or the play level during playback.
Lights during playback.
Displays the sampling frequency (Fs) of the current digital input. All indicators are off when the input signal is interrupted.
Lights when automatic track number write during recording is activated.
Displays the elapsed playing time, remaining playing time, total playing time, elapsed recording time, remaining recording time, total recording time and remaining time until the end of finalization.
Blinks during disc identification and lights steadily if the loaded disc is a CD-R disc before finalization.

14. SPECIFICATIONS

• The following dimensions are for PDR-99/KU.

1. GENERAL

Model	Compact disc audio system
Applicable discs	CDs and CD-Rs
Power supply	AC 120 V, 60 Hz
Power consumption	19 W
Operating temperature	+5 °C to +35 °C (+41 °F to +95 °F)
Weight (without package)	6 kg (13 lb 1 oz)
Max. dimensions	457 (W) x 287 (D) x 132 (H) mm 18 (W) x 11-5/16 (D) x 5-7/32 (H) in

2. AUDIO UNIT

Frequency characteristics	2 Hz to 20 kHz
Playback S/N	112 dB (EIAJ)
Playback dynamic range	97 dB (EIAJ)
Playback total harmonic distortion	0.0026 % (EIAJ)
Playback channel separation	100 dB
Recording S/N	92 dB
Recording dynamic range	92 dB
Recording total harmonic distortion	0.004 %
Output voltage	2 V
Wow-flutter	Less than measurement limit ((±0.001 % W.PEAK) (EIAJ))
Number of channels	2 channels (stereo)
Digital output	Coaxial output: 0.5 Vp-p ±20 % (75 Ω)
Optical output:	–15 to –20 dBm (wavelenght: 660 nm) Frequency deflection: Level 2 (standard mode)

* Recording specification values are for the LINE input (ANALOG).

3. INPUT JACKS

Optical digital input jacks
Coaxial digital input jack
Audio LINE input jack

4. OUTPUT JACKS

Optical digital output jack
Coaxial digital output jack
Audio LINE output jack

5. RECORDING FUNCTIONS

- Recording
- Automatic digital-source synchro recording (1-track recording)
- Automatic digital-source synchro recording (All-track recording)
- REC MUTE
- AUTO TRACK INCREMENT
- AUTO REC/PAUSE
- Remaining recording time display
- PREVIOUS
- MANUAL TRACK INCREMENT
- INPUT SELECTOR
- TOC Write
- Fade-in/fade-out
- SCMS (Serial Copy Management System)
- Sampling monitor

6. PLAYBACK FUNCTIONS

- PLAY
- PAUSE
- STOP
- MANUAL search
- TRACK search
- Direct song selection
- 1-Track repeat
- All-track repeat
- Programmed repeat
- Programmed playback (max. 24 tracks)
- Program check
- Program correction
- Program clear
- Pause programming
- Program reservation
- SKIP playback
- DISPLAY OFF
- TIME display switching
- Random playback
- Fade in/Fade out

7. ACCESSORIES

• Remote control unit (CU-PD075)	1
• Size AAA/R03 dry cell batteries	2
• Audio cable	2
• Control cable	1
• Operating Instructions	1

NOTE:
The specifications and design of this product are subject to change without notice, due to improvements.